Bibliography on Architectures for Power Management

[ABD+03] David H. Albonesi, Rajeev Balasubramonian, Steven G. Dropsho, Sandhya Dwarkadas, Eby G. Friedman, Michael C. Huang, Volkan Kursun, Grigorios Magklis, Michael L. Scott, Greg Semeraro, Pradip Bose, Alper Buyuktosunoglu, Peter W. Cook, and Stanley E. Schuster. Dynamically tuning processor resources with adaptive processing. *IEEE Computer*, 36(12):49–58, December 2003. DOI 10.1109/MC.2003.1250883

[ACM04] Raksit Ashok, Saurabh Chheda, and Csaba Andras Moritz. Coupling compiler-enabled and conventional memory accessing for energy efficiency. *ACM Transactions on Computer Systems*, 22(2):180–213, May 2004. DOI 10.1145/986533.986535

[AGS05] Murali Annavaram, Ed Grochowski, and John Shen. Mitigating Amdahl's law through EPI throttling. *SIGARCH Comput. Archit. News*, 33(2):298–309, 2005. DOI 10.1145/1080695.1069995 URL http://www.cs.wisc.edu/~isca2005/papers/05B-01.PDF

[BB95] T. D. Burd and R. W. Brodersen. Energy efficient CMOS microprocessor design. In *Proceedings of the 28th Hawaii International Conference on System Sciences (HICSS'95)*, page 288, Washington, DC, USA, 1995. IEEE Computer Society.

[BC06] Michela Becchi and Patrick Crowley. Dynamic thread assignment on heterogeneous multiprocessor architectures. In *Proceedings of the Third Conference on Computing frontiers (CF'06)*, pages 29–40, New York, NY, USA, 2006. ACM Press. DOI 10.1145/1128022.1128029

[BDK+05] Shekkar Y. Borkar, Pradeep Dubey, David J. Kuck, Hans Mulder, Stephen S. Pawlowski, and Justin R. Rattner. Platform 2015: Intel processor and platform evolution for the next decade. White Paper, Intel Corporation, 2005.

[Bel04] Frank Bellosa. When physical is not real enough. In *Proceedings of the Eleventh ACM SIGOPS European Workshop 2004*, September 2004. URL http://os.ibds.kit.edu/downloads/publ_2004_bellosa_sigops-ew04-mmc.pdf

[BR00] Michael A. Bender and Michael O. Rabin. Scheduling cilk multithreaded parallel programs on processors of different speeds. In *Proceedings of the ACM Symposium on Parallel Algorithms and Architectures*, pages 13–21, 2000. URL http://supertech.csail.mit.edu/papers/spaa00-heterogeneous.ps

[BRUL05] Saisanthosh Balakrishnan, Ravi Rajwar, Mike Upton, and Konrad Lai. The impact of performance asymmetry in emerging multicore architectures. In *Proceedings of the 32nd International Symposium on Computer Architecture (ISCA'05)*, June 2005. DOI 10.1109/ISCA.2005.51

[CBL+07] John M. Calandrino, Dan Baumberger, Tong Li, Scott Hahn, and James H. Anderson. Soft real-time scheduling on performance asymmetric multicore platforms. In *Proceedings of the Thirteenth Real-Time and Embedded Technology and Applications Symposium (RTAS'07)*, pages 101–112, Washington, DC, USA, 2007. IEEE Computer Society. DOI 10.1109/RTAS.2007.35 URL http://www.cs.unc.edu/~anderson/papers/rtas07.ps

[CJ08] Jian Chen and Lizy K. John. Energy-aware application scheduling on a heterogeneous multicore system. In *Proceedings of the IEEE International Symposium on Workload Characterization (IISWC'08)*, 2008. URL http://www.iiswc.org/iiswc2008/Papers/001.pdf

[DM04] James Donald and Margaret Martonosi. Temperature-aware design issues for SMT and CMP architectures. In *Proceedings of the Fifth Workshop on Complexity-Effective Design, in conjunction with International Symposium on Computer Architecture (ISCA)*, June 2004.

[GG03a] Soraya Ghiasi and Dirk Grunwald. Aide de Camp: Asymmetric dual core design for power and energy reduction. Technical Report 80309-0430, University of Colorado, Boulder, Department of Computer Science, May 2003. URL http://www.cs.colorado.edu/department/publications/reports/docs/CU-CS-964-03.pdf

[GG03b] José González and Antonio González. Dynamic cluster resizing. In *Proceedings of the 2003 IEEE International Conference on Computer Design (ICCD'03)*, October 2003. DOI 10.1109/ICCD.2003.1240922

[GH96] R. Gonzalez and M. Horowitz. Energy dissipation in general purpose microprocessors. *IEEE Journal of Solid-State Circuits*, 31(9):1277–1284, September 1996. URL http://www-vlsi.stanford.edu/papers/reg_jssc_9_96.pdf

[GKR05] Soraya Ghiasi, Tom Keller, and Freeman Rawson. Scheduling for heterogeneous processors in server systems. In *Proceedings of the Second Conference on Computing frontiers (CF'05)*, pages 199–210, New York, NY, USA, 2005. ACM. DOI 10.1145/1062261.1062295

[GRSW04] E. Grochowski, R. Ronen, J. Shen, and H. Wang. Best of both latency and throughput. In *Proceedings of the 2004 IEEE International Conference on Computer Design (ICCD'04)*, pages 236 – 243, October 2004. DOI 10.1109/ICCD.2004.1347928

[HKS+03] J. Haid, G. Kaefer, Ch. Steger, R. Weiss, W. Schögler, and M. Manninger. Run-time energy estimation in system-on-a-chip designs. In *Proceedings of the Eighth Asia and South Pacific Design Automation Conference (ASP-DAC'03)*, pages 595–599, January 2003. DOI 10.1109/ASPDAC.2003.1195094

[HS99] P. Havinga and G. Smit. Octopus: embracing the energy efficiency of handheld multimedia computers. In *Proceedings of the Fifth Annual International Conference on Mobile Computing and Networking (MOBICOM'99)*, August 1999. URL http://www.acm.org/pubs/articles/proceedings/comm/313451/p77-havinga/p77-havinga.pdf

[HSWV01] P. Havinga, G. Smit, G. Wu, and L. Vognild. Energy management for dynamically reconfigurable heterogeneous mobile systems. In *Proceedings of the 10th Heterogeneous Computing Workshop*, April 2001. URL http://wwwhome.cs.utwente.nl/~havinga/papers/havinga_hcw01.pdf

[Jha01] Niraj K. Jha. Low power system scheduling and synthesis. In *Proceedings of the International Conference on Computer-Aided Design (ICCAD'01)*, pages 259–263, Piscataway, NJ, USA, 2001. IEEE Press.

[KAB+03] Nam Sung Kim, Todd Austin, David Blaauw, Trevor Mudge, Krisztián Flautner, Jie S. Hu, Mary Jane Irwin, Mahmut Kandemir, and Vijaykrishnan Narayanan. Leakage current: Moore's law meets static power. *IEEE Computer*, 36(12):68–75, December 2003. DOI 10.1109/MC.2003.1250885

[KAMG02] N. Kim, T. Austin, T. Mudge, and D. Grunwald. Challenges for architectural level power modeling. In Robert Graybill and Rami Melhem, editors, *Power Aware Computing*. Kluwer Academic Publishers, 2002. URL http://www.eecs.umich.edu/~tnm/papers/challenges.pdf

[KEPA08] Theodoros Konstantakopoulos, Jonathan Eastep, James Psota, and Ananth Agarwal. Energy scalability of on-chip interconnection networks in multicore architecture. Technical report, Massachusetts Institute of Technology, 2008.

[KFBM02] Nam Sung Kim, Krisztián Flautner, David Blaauw, and Trevor Mudge. Drowsy instruction caches: leakage power reduction using dynamic voltage scaling and cache sub-bank prediction. In *Proceedings of the 35th International Symposium on Microarchitecture MICRO'2002*, December 2002. URL http://www.eecs.umich.edu/~tnm/papers/micro02.pdf

[KFJ+03] Rakesh Kumar, Keith I. Farkas, Norman P. Jouppi, Parthasarathy Ranganathan, and Dean M. Tullsen. Single-ISA heterogeneous multi-core architectures: The potential for processor power reduction. In *Proceedings of the 36th Annual IEEE/ACM International Symposium on Microarchitecture (MIRCO'03)*, 2003.

[KGWB08] Wonyoung Kim, Meeta S. Gupta, Gu-Yeon Wei, and David Brooks. System level analysis of fast, per-core dvfs using on-chip switching regulators. In *Proceedings of the Fourteenth International Symposium on High-Performance Computer Architecture (HPCA'08)*, February 2008. URL http://www.eecs.harvard.edu/~dbrooks/kim2008_hpca.pdf

[KTJ06] Rakesh Kumar, Dean M. Tullsen, and Norman P. Jouppi. Core architecture optimization for heterogeneous chip multiprocessors. In *Proceedings of the Fifteenth Conference on Parallel Architectures and Compilation Techniques (PACT'06)*, pages 23–32, New York, NY, USA, 2006. ACM. DOI 10.1145/1152154.1152162 URL http://www-cse.ucsd.edu/users/tullsen/pact06.pdf

[KTR+04] Rakesh Kumar, Dean M. Tullsen, Parthasarathy Ranganathan, Norman P. Jouppi, and Keith I. Farkas. Single-ISA heterogeneous multi-core architectures for multithreaded workload performance. In *Proceedings of the 31st International Symposium on Computer Architecture (ISCA'04)*, pages 64–75, June 2004. URL http://passat.crhc.illinois.edu/rakeshk/multicore_isca04.pdf

[KZT05] Rakesh Kumar, Victor Zyuban, and Dean M. Tullsen. Interconnections in multi-core architectures: Understanding mechanisms, overheads and scaling. *SIGARCH Comput. Archit. News*, 33(2):408–419, 2005. DOI 10.1145/1080695.1070004

[LH01] Weiping Liao and Lei He. Power modeling and reduction of VLIW processors. In *Proceedings of the Workshop on Compilers and Operating Systems for Low Power (COLP'01)*, September 2001. URL http://research.ac.upc.es/pact01/colp/paper08.pdf

[LHO97] B. Nayfeh L. Hammond and K. Olukotun. A single-chip multiprocessor. *IEEE Computer*, 30(9):79–85, September 1997. DOI 10.1109/2.612253

[LY74] Jane W. S. Liu and Ai-Tsung Yang. Optimal scheduling of independent tasks on heterogeneous computing systems. In *ACM 74: Proceedings of the 1974 annual conference*, pages 38–45, New York, NY, USA, 1974. ACM Press. DOI 10.1145/800182.810377

[MPB+06] R. McGowen, C.A. Poirier, C. Bostak, J. Ignowski, M. Millican, W.H. Parks, and S. Naffziger. Power and temperature control on a 90-nm itanium family processor. *Solid-State Circuits, IEEE Journal of*, 41(1):229–237, January 2006. DOI 10.1109/JSSC.2005.859902

[Mud01] Trevor Mudge. Power: A first-class architectural design constraint. *IEEE Computer*, April 2001. DOI 10.1109/2.917539

[MWK04] Tomer Morad, Uri Weiser, and Avnoam Kolody. ACCMP — asymmetric cluster chip multiprocessing. Technical report, CCIT, 2004. URL http://www.ee.technion.ac.il/people/morad/publications/accmptr.pdf

[MWK+06] Tomer Y. Morad, Uri C. Weiser, Avinoam Kolodny, Mateo Valero, and Eduard Ayguade. Performance, power efficiency and scalability of asymmetric cluster chip multiprocessors. *IEEE Comput. Archit. Lett.*, 5(1):14–17, 2006. DOI 10.1109/L-CA.2006.6 URL http://www.ee.technion.ac.il/matrics/papers/Performance,%20Power%20Efficiency%20and%20Scalability%20of%20Asymmetric%20Cluster%20Chip%20Multiprocessors.pdf

[NCB03] K. J. Nowka, G. D. Carpenter, and B. C. Brock. The design and application of the PowerPC 405LP energy-efficient system-on-a-chip. *IBM Journal of Research and Development*, 47(5):632–639, 2003. DOI 10.1147/rd.475.0631

[ONH+97] Kunle Olukotun, Basem Nayfeh, Lance Hammond, Ken Wilson, and Kunyung Chang. The case for a single-chip multiprocessor. In *Proceedings of the Seventh International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS'97)*, October 1997. DOI 10.1145/237090.237140

[PMSD04] Eric Piel, Philippe Marquet, Julien Soula, and Jean-Luc Dekeyser. Load-balancing for a real-time system based on asymmetric multi-processing. In *Proceedings of the Sixteenth Euromicro Conference on Real-Time Systems*, Catania, Italy, June 2004. URL http://www2.lifl.fr/west/publi/PMSD04ecrts.pdf

[RP05] Peng Rong and Massoud Pedram. Hierarchical power management with application to scheduling. In *Proceedings of the 2005 International Symposium on Low-Power Electronics and Design (ISLPED'05)*, pages 269–274, New York, NY, USA, August 2005. ACM Press. DOI 10.1145/1077603.1077667

[SB02] T. Simunic and S. Boyd. Managing power consumption in networks on chip. In *Proceedings of the Conference on Design Automation and Test in Europe (DATE'02)*, 2002. URL http://www.date-conference.com/proceedings/PAPERS/2002/DATE02/pdffiles/01e_2.pdf

[SBCR05] Jacob Sorber, Nilanjan Banerjee, Mark D. Corner, and Sami Rollins. Turducken: hierarchical power management for mobile devices. In *Proceedings of the Third International Conference on Mobile Systems, Applications, and Services (MOBISYS'05)*, June 2005. DOI 10.1145/1067170.1067198

[SMHK02] P. Stanley-Marbell, M. Hsiao, and U. Kremer. A hardware architecture for dynamic performance and energy adaption. In *Proceedings of the Workshop on Power-Aware Computer Systems (PACS'02)*, February 2002. URL http://www.cs.rutgers.edu/~uli/PACS02-pau.ps

[SPM05] Ruresh Siddha, Venkatesh Pallipadi, and Asit Mallick. Chip multi processing aware linux kernel scheduler. In *Proceedings of the 2005 Linux Symposium*, 2005.

[SSB+03] M.R. Stan, K. Skadron, M. Barcella, W. Huang, K. Sankaranarayanan, , and S. Velusamy. Hotspot: A dynamic compact thermal model at the processor-architecture level. *Microelectronics Journal: Circuits and Systems*, 34(12):1153–1165, December 2003. URL http://www.cs.virginia.edu/~skadron/Papers/hotspot_mej.pdf

[STC00] John S. Seng, Dean M. Tullsen, and George Z.N. Cai. Power-sensitive multithreaded architecture. *Proceedings of the 2000 IEEE International Conference on Computer Design (ICCD'00)*, 00:199–206, September 2000. DOI 10.1109/ICCD.2000.878286

[UU04] S. Uhrig and Th. Ungerer. Fine-grained power management for real-time embedded processors. In *Proceedings of the 12th International Conference on Real-Time Systems RTS'04*, March 2004. URL http://ipr.ira.uka.de/komodo/publications/RTS04.pdf