Concurrent Systems

Nebenläufige Systeme

XIV. Pickings

Wolfgang Schröder-Preikschat

February 5, 2019

Agenda

Recapitulation
- Concurrent Systems

Perspectives
- Parallel Systems
- Computing Equipment
- Further Education

Outline

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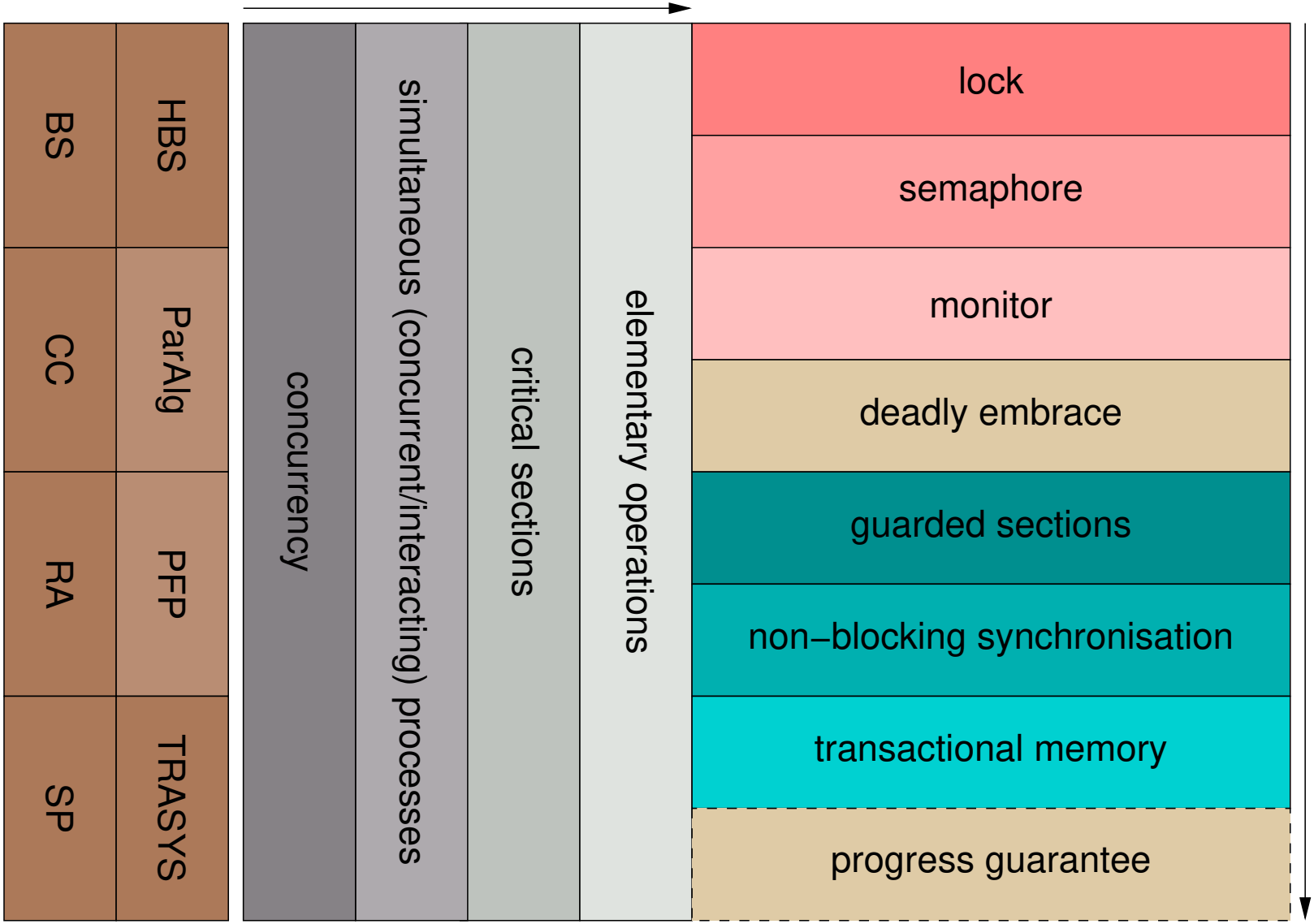
Content of Teaching and Cross-References



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Main Research at the Chair

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  - application-oriented (varying, type-safe) system software
- **specialisation**
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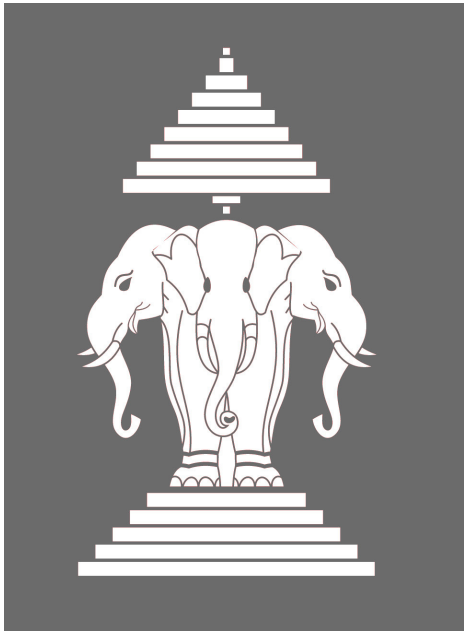
↪ "concurrent systems" is more or less **cross-cutting** thereto...

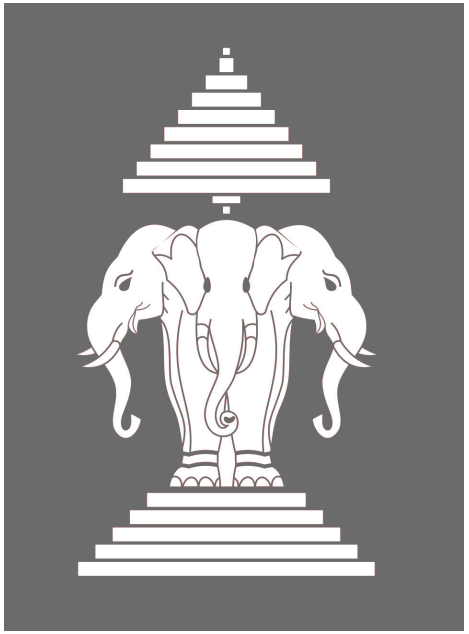
Latency Awareness in Operating Systems



[1] http://univis.uni-erlangen.de → Research projects → LAOS

Latency Awareness in Operating Systems

- **latency prevention**
  - lock- and wait-free synchronisation
  - integrated generator-based approach
- **latency avoidance**
  - interference protection
  - race-conflict containment
- **latency hiding**
  - operating-system server cores
  - asynchronous remote system operation



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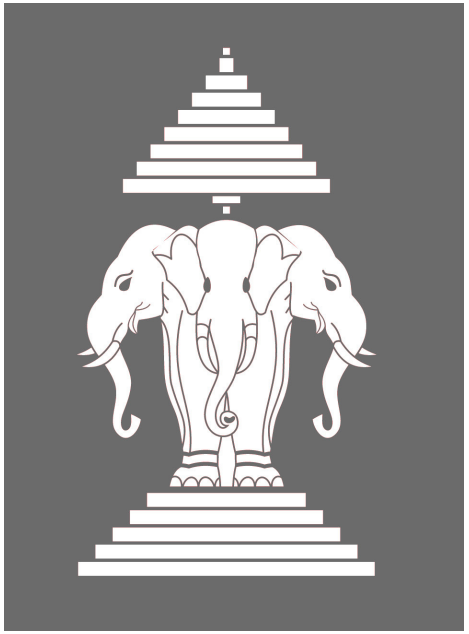

- experiments with different **operating-system architectures**
  - process-/event-based and hardware-centric operating-system kernels
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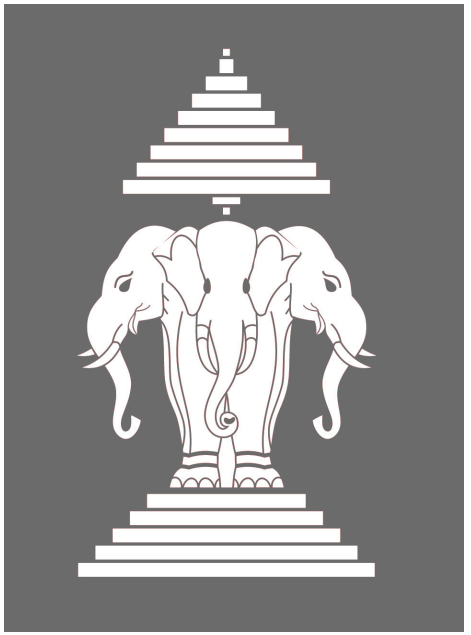

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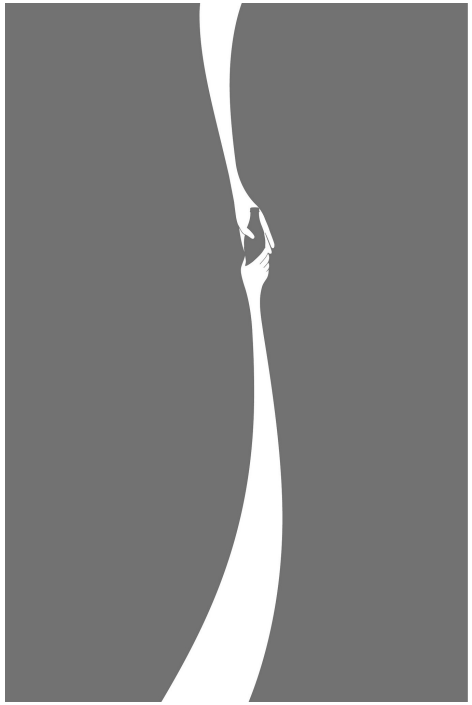
Coherency Kernel



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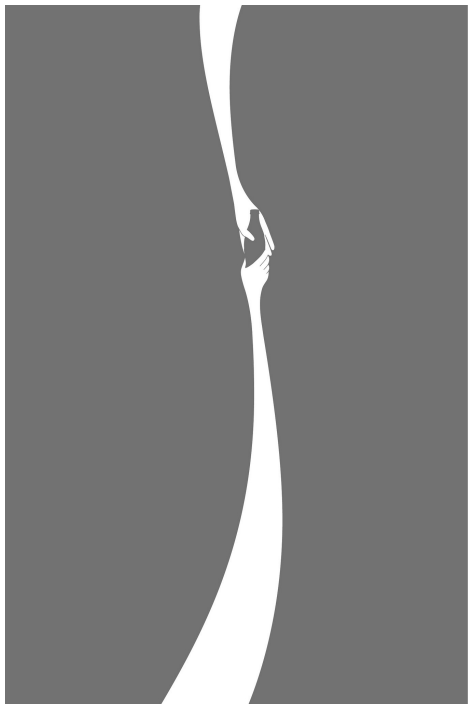
  - cache-aware main-memory footprint
  - hyper-threading of latent actions



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  - memory domains for NUMA architectures

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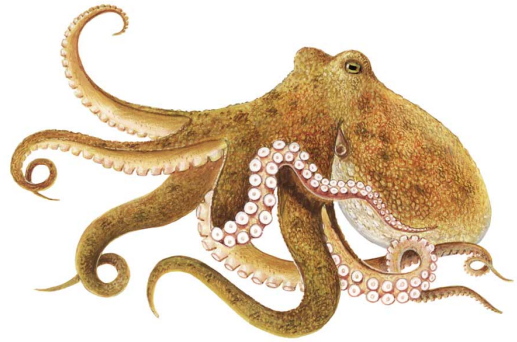
Run-Time Support System for Invasive Computing



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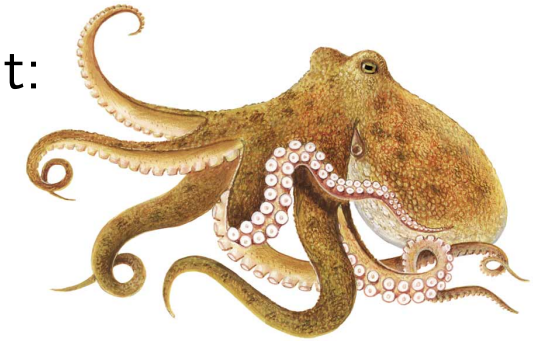
Run-Time Support System for Invasive Computing

Octo



- borrowed from the designation of a creature that:
  - i is highly parallel in its actions and
  - ii excellently can adapt oneself to its environment
- the kraken (species *Octopoda*)
  - can operate in parallel by virtue of its eight tentacle
  - is able to do customisation through camouflage and deimatic displays and
  - comes with a highly developed nervous system
    - in order to attune to dynamic ambient conditions and effects

POS

- abbrv. for *parallel operating system*
  - an operating system that not only supports parallel processes
  - but that also functions inherently parallel thereby

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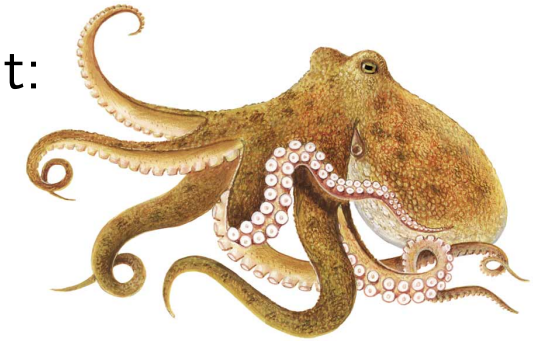

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Power-Aware Critical Sections

PAX

[4] `http://univis.uni-erlangen.de` → Research projects → PAX

Power-Aware Critical Sections

- scalable synchronisation on the basis of **agile critical sections**
  - infrastructure
    - load-dependent and self-organised change of protection against race conditions
  - linguistic support
    - preparation, characterisation, and capturing of declared critical sections

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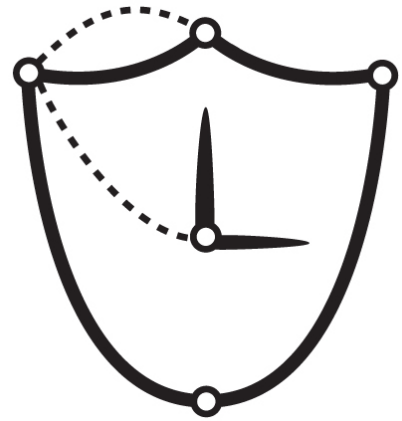
Latency- and Resilience-Aware Networking



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  - transport channel for cyber-physical systems
  - predictable transmission latency
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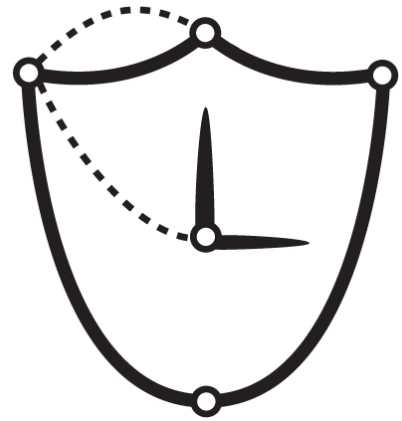

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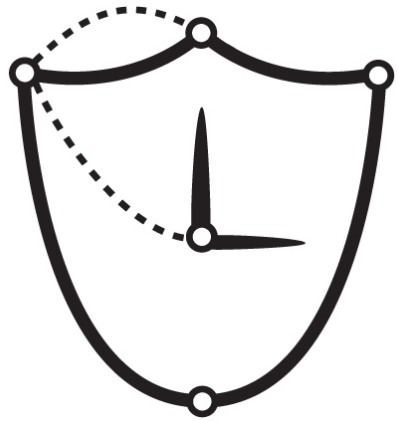

- **deterministic run-time support**

  Auffassung von der kausalen [Vor]bestimmtheit allen Geschehens bzw. Handelns (Duden)

  - latency-aware communication endpoints, optimised protocol stack
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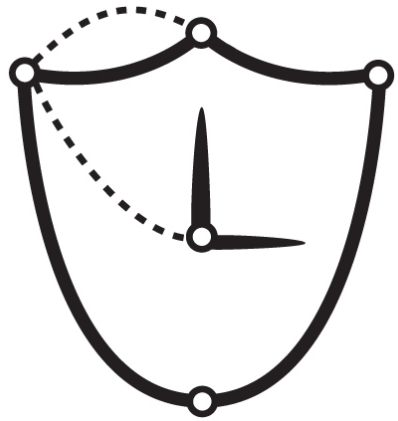

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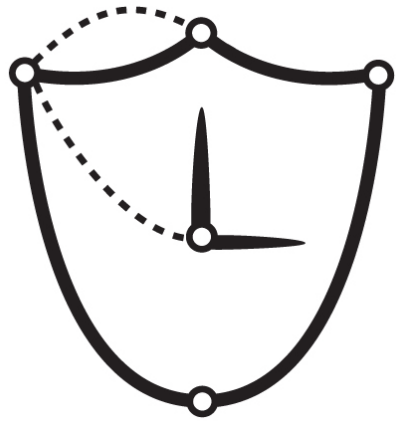

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Multi/Many-Core Processor Pool

faui4*	clock	cores per domain		domain		
		physical	logical	NUMA	tile	
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9big01	2.5 GHz	6	–	8	–	Opteron
9big02	2.2 GHz	10	20	4	–	Xeon
9phi01	1.2 GHz	6	12	2	–	Xeon
	1.1 GHz	57	228	2	–	Xeon Phi
scc	1.5 GHz	4	2	1	–	Xeon
	800 MHz	2	–	–	24	Pentium
InvasIC	3.5 GHz	8	16	2	–	Xeon
	25 MHz	4	–	6		LEON/SPARC

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- budgeted acquisition: further n-core systems, transactional memory

OctoPOS
- $n \geq 64$

PAX
- $n \geq 16$, plus several multi-core micro-controllers

Bachelor, Master, or Doctoral Thesis