Concurrent Systems

Nebenläufige Systeme

XIV. Pickings

Wolfgang Schröder-Preikschat

February 11, 2021

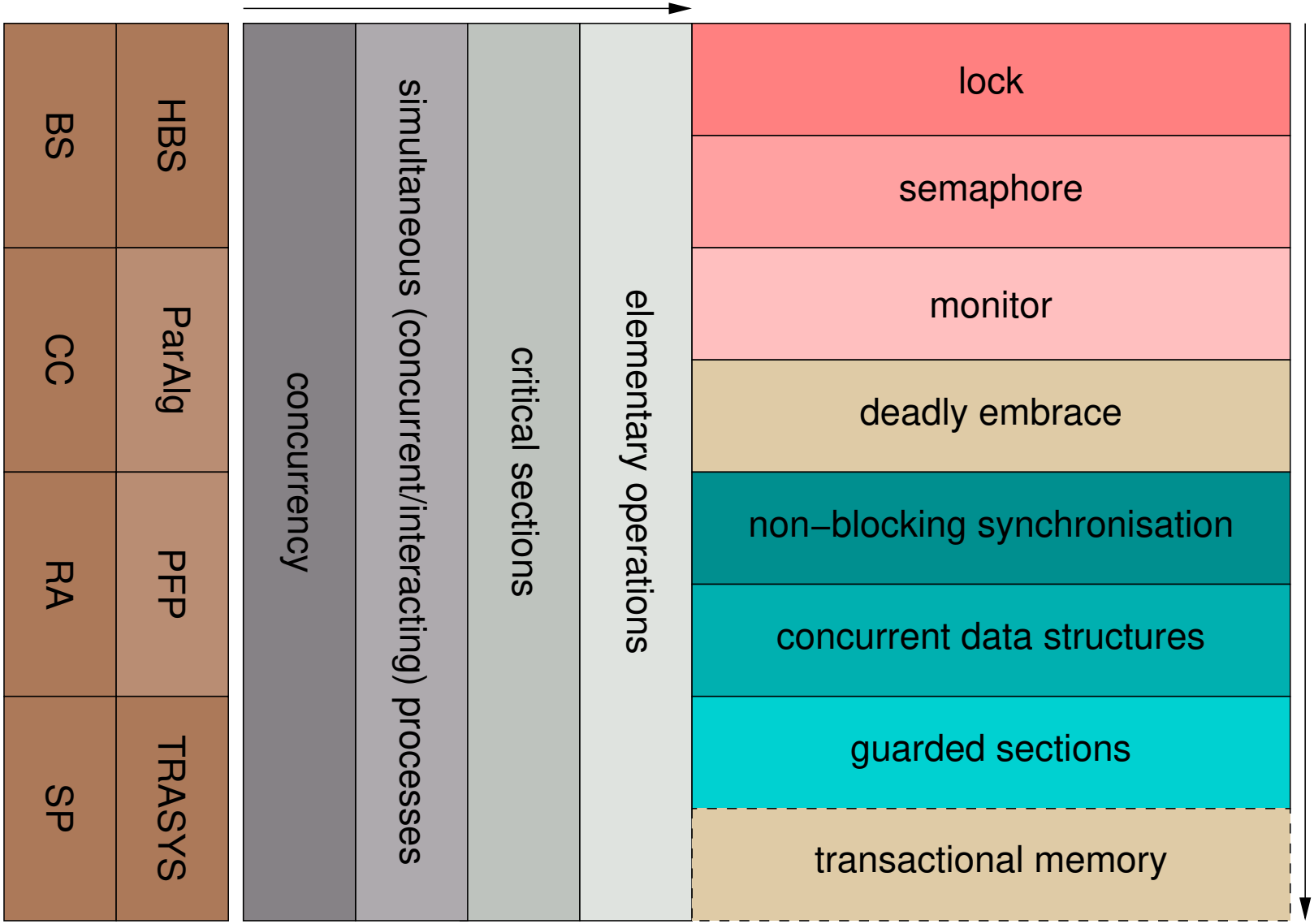
Agenda

Recapitulation
- Concurrent Systems

Perspectives
- Parallel Systems
- Computing Equipment
- Further Education

Outline

Content of Teaching and Cross-References



Outline

Main Research at the Chair

- **composability** and **configurability**
  - application-oriented (varying, type-safe) system software
- **specialisation**
  - dedicated operating systems: integrated, adaptive, parallel

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- **reliability**
  - gentle fault and intrusion tolerance
- **thriftiness**
  - resource-aware operation of computing systems
- **timeliness**
  - migration paths between time- and event-triggered real-time systems

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- **concurrency**
  - coordination of cooperation and competition between processes

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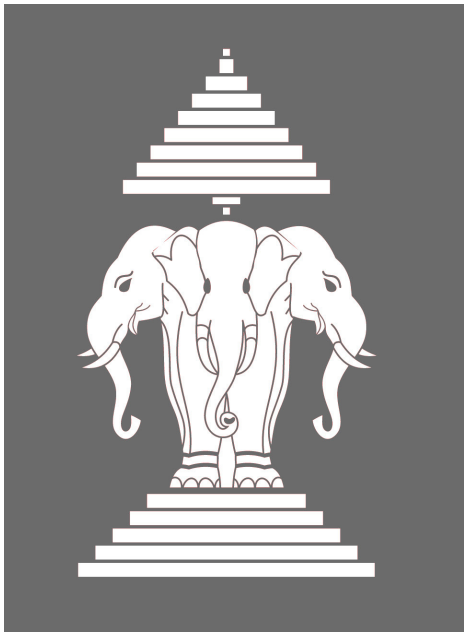
↪ "concurrent systems" is more or less **cross-cutting** thereto...

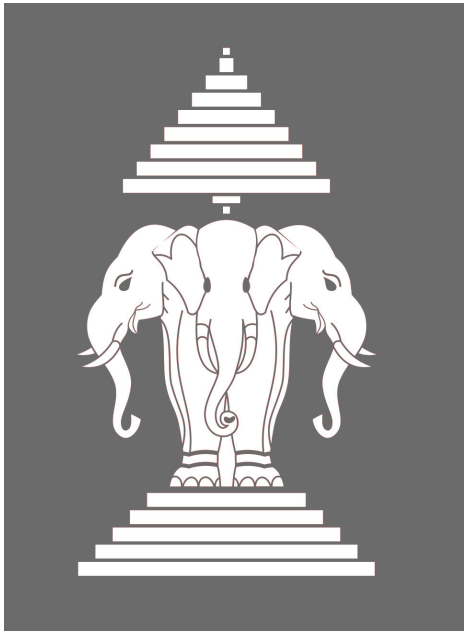
Latency Awareness in Operating Systems



[1] http://univis.uni-erlangen.de → Research projects → LAOS

Latency Awareness in Operating Systems

- **latency prevention**
  - lock- and wait-free synchronisation
  - integrated generator-based approach
- **latency avoidance**
  - interference protection
  - race-conflict containment
- **latency hiding**
  - operating-system server cores
  - asynchronous remote system operation



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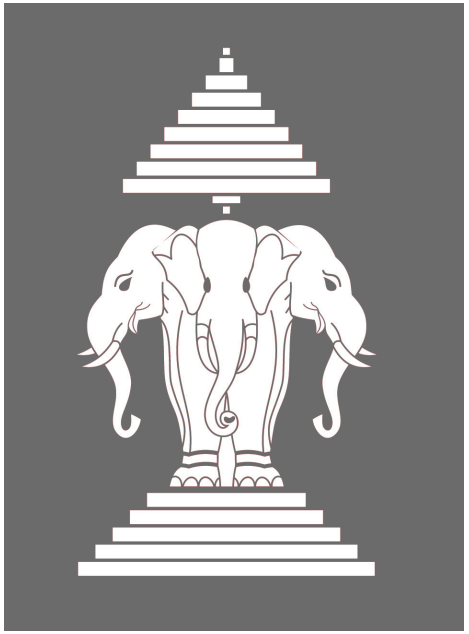

- experiments with different **operating-system architectures**
  - process-/event-based and hardware-centric operating-system kernels
  - LAKE, Sloth

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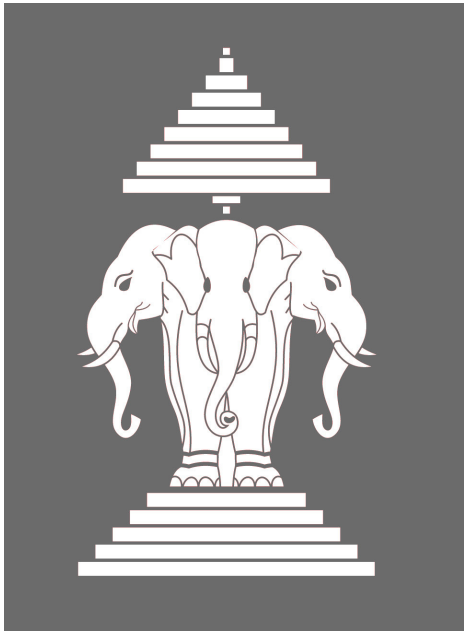

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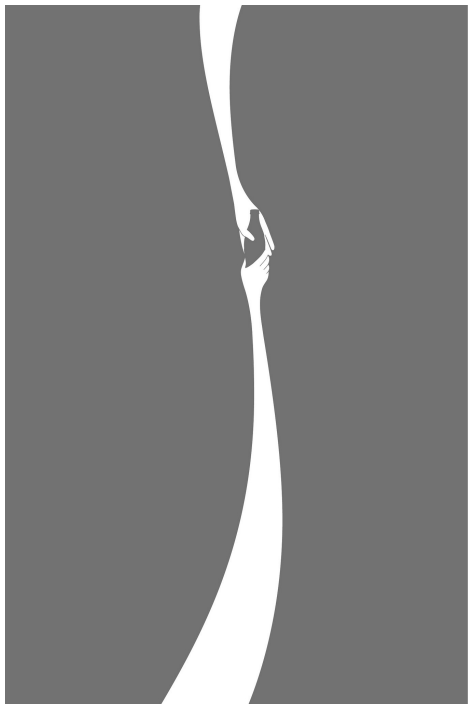
Coherency Kernel



[2] http://univis.uni-erlangen.de → Research projects → COKE

Coherency Kernel

- **event-based minimal kernel**
  - cache-aware main-memory footprint
  - hyper-threading of latent actions

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Power-Aware Critical Sections

PAX

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Power-Aware Critical Sections

- scalable synchronisation on the basis of **agile critical sections**
  - infrastructure
    - load-dependent and self-organised change of protection against race conditions
  - linguistic support
    - preparation, characterisation, and capturing of declared critical sections

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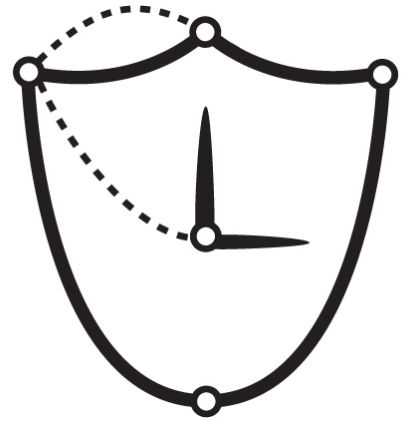
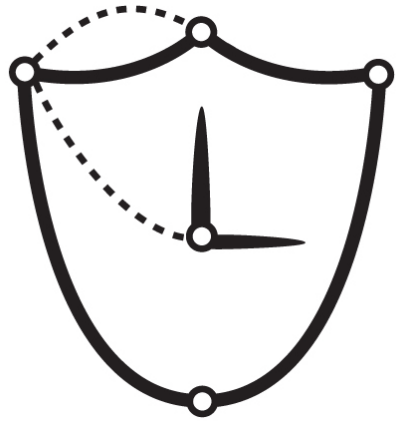
Latency- and Resilience-Aware Networking



[4] http://univis.uni-erlangen.de → Research projects → LARN

Latency- and Resilience-Aware Networking

- **real-time capable network communication**
  - transport channel for cyber-physical systems
  - predictable transmission latency
  - in a certain extent guaranteed quality criteria



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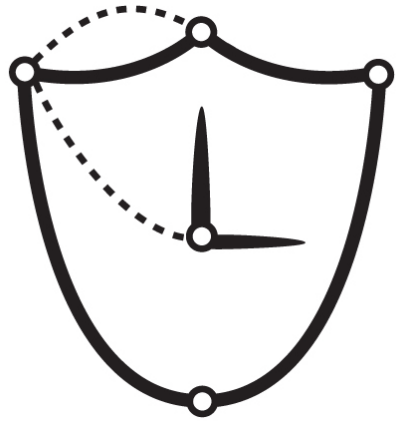

- **deterministic run-time support**

  Auffassung von der kausalen [Vor]bestimmtheit allen Geschehens bzw. Handelns (Duden)

  - latency-aware communication endpoints, optimised protocol stack
  - specialised resource management, predictable run-time behaviour

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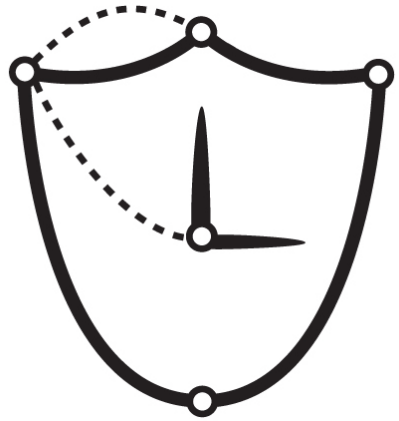

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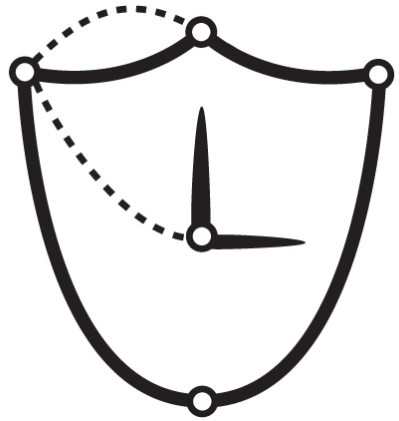

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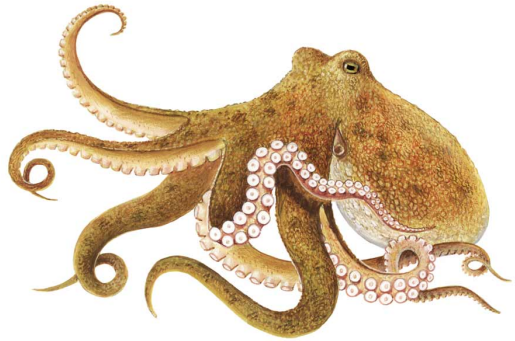
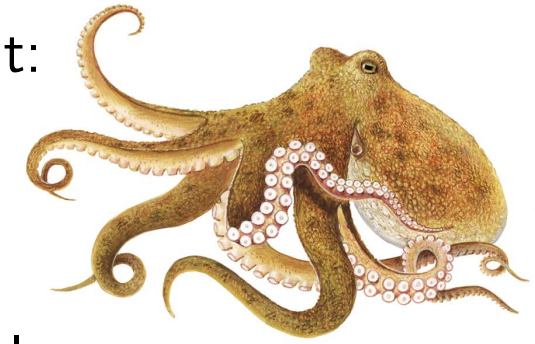
Run-Time Support System for Invasive Computing



[5] http://univis.uni-erlangen.de → Research projects → iRTSS

Run-Time Support System for Invasive Computing

Octo



- borrowed from the designation of a creature that:
  - i is highly parallel in its actions and
  - ii excellently can adapt oneself to its environment
- the kraken (species *Octopoda*)
  - can operate in parallel by virtue of its eight tentacle
  - is able to do customisation through camouflage and deimatic displays and
  - comes with a highly developed nervous system
    - in order to attune to dynamic ambient conditions and effects

POS

- abbrv. for *parallel operating system*
  - an operating system that not only supports parallel processes
  - but that also functions inherently parallel thereby

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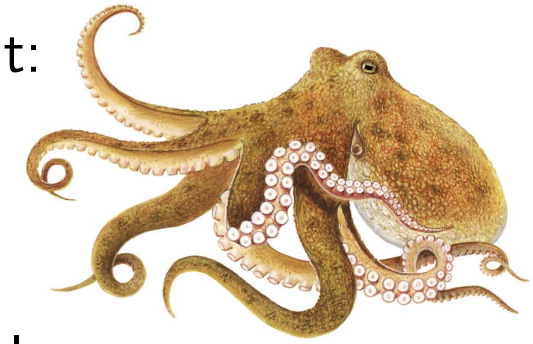

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Multi/Many-Core Processor Pool

faui4*	clock	cores per domain		domain		#	
		physical	logical	NUMA	tile		
*8e *8f	2.9 GHz	8	16	2	1	32	Xeon
*9big01	2.5 GHz	6	6	8	1	48	Opteron
*9big02	2.2 GHz	10	20	4	1	80	Xeon
*9big03	2.1 GHz	12	24	4	1	96	Xeon
*9big04	2 GHz[6]	64	128	2	1	256	Epyc
*9big05	2.5 GHz	16	128	2	4	1024	ThunderX2
*9phi01	1.2 GHz	6	12	2	1	24	Xeon
	1.1 GHz	57	228	2	1	456	Xeon Phi
*scc	1.5 GHz	4	8	1	1	8	Xeon
	800 MHz	2	–	–	24	48	Pentium
fastbox	3.5 GHz	4	8	1	1	8	Xeon TSX
InvasIC	50 MHz	5	5	16		80	LEON/SPARC
						2160	

[6] mit *boost* 3.35 GHz

Bachelor, Master, or Doctoral Thesis