Konfigurierbare Systemsoftware (KSS)

VL 6 – Generative Programming: The SLOTH Approach

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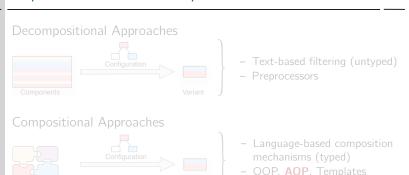
Friedrich-Alexander-Universität Erlangen-Nürnberg

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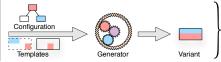


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Implementation Techniques: Classification



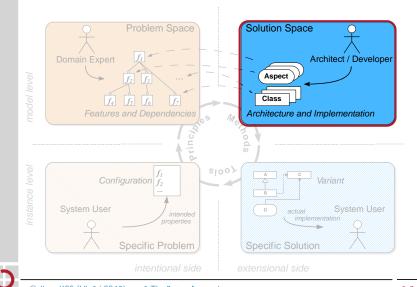
Generative Approaches



- Metamodel-based generation of components (typed)
- MDD. C++ TMP. generators

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About this Lecture

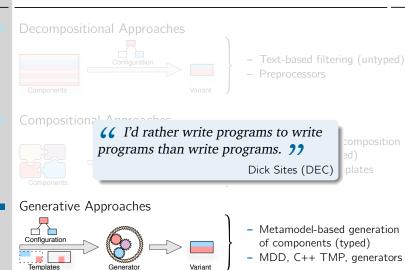


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6 The SLOTH Approach

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Implementation Techniques: Classification



Agenda

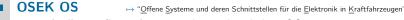
- 6.1 Motivation: OSEK and Co 6.2 **SLOTH**: Threads as Interrupts
- 6.3 SLEEPY SLOTH: Threads as IRQs as Threads 6.4 SLOTH ON TIME: Time-Triggered Laziness
- 6.5 **SLOTH*** Generation
- 6.6 Summary and Conclusions
- 6.7 References



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The OSEK Family of Automotive OS Standards

- 1995 OSEK OS (OSEK/VDX)
- [10]
- 2001 OSEKtime (OSEK/VDX)
- **2005** AUTOSAR OS (AUTOSAR)
- [1]



- **statically configured**, event-triggered real-time OS
- **OSEKtime**
 - **statically configured**, time-triggered real-time OS
 - can optionally be extended with OSEK OS (to run in slack time)
- **AUTOSAR OS** → "Automotive Open System Architecture"
 - **statically configured**, event-triggered real-time OS
 - real superset of OSEK OS ~> backwards compatible
 - additional time-triggered abstractions (schedule tables, timing protection)
 - intended as a successor for both OSEK OS and OSEKtime



6.1 Motivation: OSEK and Co.

Background

OSEK OS: Abstractions

OSEK OS: Tailoring and Generation

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OSEK OS: Abstractions [8]

- Control flows
 - Task: software-triggered control flow (strictly priority-based scheduling)
 - Basic Task (BT)

run-to-completion task with strictly stack-based

- activation and termination
- Extended Task (ET) may suspend and resume execution (\mapsto coroutine)
- ISR: hardware-triggered control flow (hardware-defined scheduling)
 - Cat 1 ISR (ISR1)

runs below the kernel, may not invoke system services (\mapsto prologue without epilogue)

- Cat 2 ISR (ISR2)
- synchronized with kernel, may invoke system services (→ epilogue without prologue)
- Hook: OS—triggered signal/exception handler
 - ErrorHook - StartupHook

invoked in case of a syscall error invoked at system boot time



OSEK OS: Abstractions [8] (Cont'd)

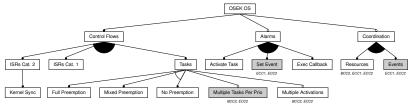
- Coordination and synchronization
 - Resource: mutual exclusion between well-defined set of tasks
 - stack-based priority ceiling protocol ([11]): GetResource() → priority is raised to that of highest participating task
 - pre-defined RES_SCHED has highest priority (~ blocks preemption)
 - implementation-optional: task set may also include cat 2 ISRs
 - Event: condition variable on which ETs may block
 - part of a task's context
 - Alarm: asynchronous trigger by HW/SW counter
 - may execute a callback, activate a task, or set an event on expiry



6 The SLOTH Approach | 6.1 Motivation: OSEK and Co

OSEK OS: Conformance Classes [8]

- OSEK offers predefined tailorability by four **conformance classes**
 - BCC1 only basic tasks, limited to one activation request per task and one task per priority, while all tasks have different priorities
 - BCC2 like BCC1, plus more than one task per priority possible and multiple requesting of task activation allowed
 - ECC1 like BCC1, plus extended tasks
 - ECC2 like ECC1, plus more than one task per priority possible and multiple requesting of task activation allowed for basic tasks
- The OSEK feature diagram





```
■ Task-related services
```

```
ActivateTask(task)
                                \rightarrow task is active (\rightarrow ready), counted
- TerminateTask()

→ running task is terminated

- Schedule()

→ active task with highest priority is running

                                              ActivateTask(task)
- ChainTask(task)
                                              TerminateTask()
```

Resource-related services

```
GetResource(res)

→ current task has res ceiling priority

ReleaseResource(res)
```

■ Event-related services (extended tasks only!)

```
SetEvent(task, mask)

→ events in mask for task are set

ClearEvent(mask)

→ events in mask for current task are unset.

WaitEvent(mask)
                         until event from mask has been set
```

Alarm-related services

```
- SetAbsAlarm(alarm, ...)

→ arms alarm with absolute offset

- SetRelAlarm(alarm, ...) → arms alarm with relative offset
```

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OSEK OS: System Specification with OIL [9]

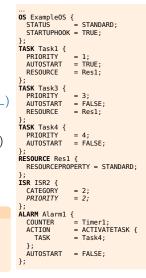
An OSEK OS instance is configured completely statically

- all general OS features (hooks. ...)
- all instances of OS abstractions (tasks, ...)
- all relationships between OS abstractions
- described in a domain-specific language (DSL)

OIL: The OSEK Implementation Language

- standard types and attributes (TASK, ISR, ...)
- vendor/plattform-specific attributes (ISR source, priority, triggering)
- task types and conformance class is deduced

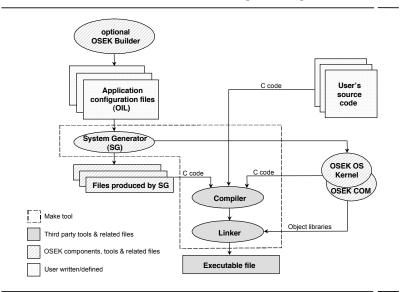
- Three basic tasks: Task1, Task3, Task4
- Category 2 ISR: ISR2 (platform-spec. source/priority)
- Task1 and Task3 use resource Res1 → ceiling pri = 3
- Alarm Alarm1 triggers Task4 on expiry





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OSEK OS: System Generation [9, p. 5]





6 The SLOTH Approach | 6.1 Motivation: OSEK and Co

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- 6.2 **SLOTH**: Threads as Interrupts

Basic Idea Design

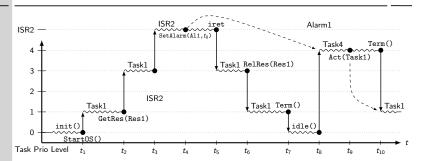
Results

Limitation

OSEK OS: Example Control Flow







- Basic tasks behave much like IRQ handlers. (on a system with support for IRQ priority levels)
 - priority-based dispatching with run-to-completion
 - LIFO, all control flows can be executed on a single shared stack
- So why not dispatch tasks as ISRs?
 - → Let the hardware do all scheduling!
 - → Let's be a Sloth!



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"SLOTH: Threads as Interrupts"

[5]

Idea: threads are interrupt handlers, synchronous thread activation is IRQ

Paper title of [5] is a pun to the approach taken by SOLARIS: "Interrupts as Threads", ACM OSR (1995) [7]

- Let interrupt subsystem do the scheduling and dispatching work
- Applicable to priority-based real-time systems
- Advantage: small, fast kernel with unified control-flow abstraction

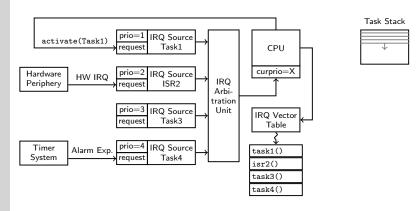






SLOTH Design

■ IRQ system must support priorities and software triggering





6 The SLOTH Approach | 6.2 SLOTH: Threads as Interrupts

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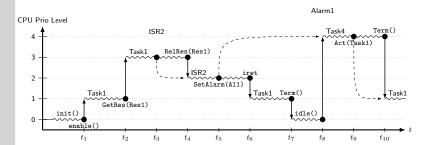
6 The SLOTH Approach | 6.2 SLOTH: Threads as Interrupts

SLOTH: Qualitative Results

- Concise kernel design and implementation
 - < 200 LoC, < 700 bytes code memory, very little RAM</p>
- Single control-flow abstraction for tasks, ISRs (1/2), callbacks
 - Handling oblivious to how it was triggered (by hardware or software)
- Unified priority space for tasks and ISRs
 - No rate-monotonic priority inversion [2, 3]
- Straight-forward synchronization by altering CPU priority
 - Resources with ceiling priority (also for ISRs!)
 - Non-preemptive sections with RES_SCHEDULER (highest task priority)
 - Kernel synchronization with highest task/cat.-2-ISR priority

SLOTH: Example Control-Flow





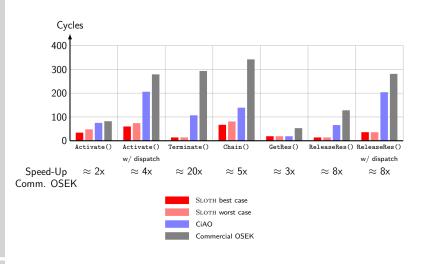


Performance Evaluation: Methodology

- Reference implementation for Infineon TriCore
 - 32-bit load/store architecture
 - Interrupt controller: 256 priority levels, about 200 IRQ sources with memory-mapped registers
 - Meanwhile also implementations for ARM Cortex-M3 (SAM3U) and x86
- Evaluation of task-related system calls:
 - Task activation
 - Task termination
 - Task acquiring/releasing resource
- Comparison with commercial OSEK implementation and CiAO
- Two numbers for SLOTH: best case, worst case
 - Depending on number of tasks and system frequency



Performance Evaluation: Results





6 The SLOTH Approach | 6.2 SLOTH: Threads as Interrupts

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6 The SLOTH Approach | 6.2 SLOTH: Threads as Interrupts

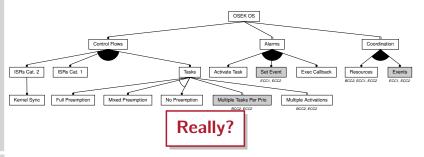
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- 6.3 SLEEPY SLOTH: Threads as IRQs as Threads

Motivation Design Results

Limitations of the SLOTH Approach

- No extended tasks (that is, events, → OSEK ECC1 / ECC2)
 - ← impossible with stack-based IRQ execution model
- No multiple tasks per priority (→ OSEK BCC2 / ECC2) execution order has to be the same as activation order



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Control Flows in Embedded Systems

	Activation Event	Sched./Disp.	Semantics
ISRs	HW	by HW	RTC
Threads	SW	by OS	Blocking
SLOTH [5]	HW or SW	by HW	RTC
SLEEPY SLOTH [6]	HW or SW	by HW	RTC or Blocking

(RTC: Run-to-Completion)





SLEEPY SLOTH: Main Goal and Challenge

Main Goal

Support extended blocking tasks (with stacks of their own), while preserving SLOTH's latency benefits by having threads run as ISRs

Main Challenge

IRQ controllers do not support suspension and re-activation of ISRs



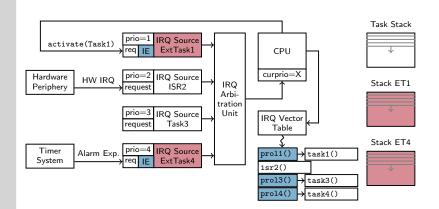
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SLEEPY SLOTH: Dispatching and Rescheduling

- Task prologue: switch stacks if necessary
 - Switch basic task → basic task omits stack switch
 - On iob start: initialize stack
 - On job resume: restore stack
- Task termination: task with next-highest priority needs to run
 - Yield CPU by setting priority to zero
 - (Prologue of *next* task performs the stack switch)
- Task blocking: take task out of "ready list"
 - Disable task's IRQ source
 - Yield CPU by setting priority to zero
- Task unblocking: put task back into "ready list"
 - Re-enable task's IRQ source
 - Re-trigger task's IRQ source by setting its pending bit



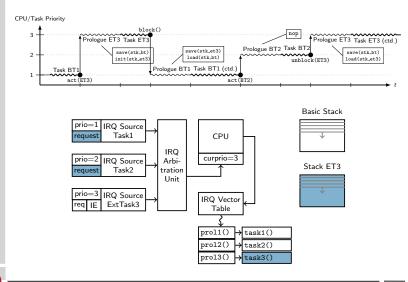
SLEEPY SLOTH Design: Task Prologues and Stacks





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SLEEPY SLOTH: Example Control Flow





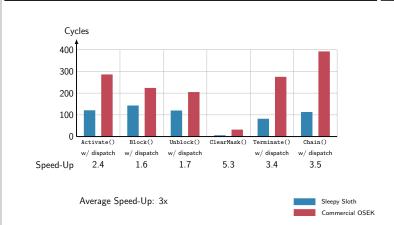
SLEEPY SLOTH: Evaluation

- Reference implementation on Infineon TriCore microcontroller
- Measurements: system call latencies in 3 system configurations, compared to a leading commercial OSEK implementation
 - 1. Only basic run-to-completion tasks
 - 2. Only extended blocking tasks
 - 3. Both basic and extended tasks



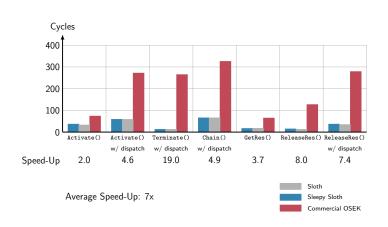
6 The SLOTH Approach | 6.3 SLEEPY SLOTH: Threads as IRQs as Threads 6–28

Evaluation: Only Extended Tasks



- Still faster than commercial kernel with SW scheduler
- SLEEPY SLOTH: Extended switches slower than basic switches

Evaluation: Only Basic Tasks

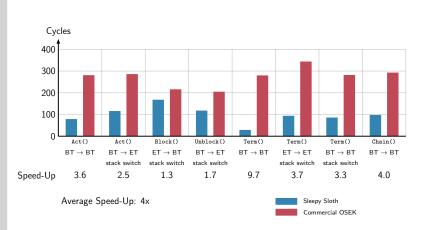


- SLEEPY SLOTH outperforms commercial kernel with SW scheduler
 - SLEEPY SLOTH as fast as original SLOTH



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Evaluation: Extended and Basic Tasks



Basic switches in a mixed system only slightly slower than in purely basic system



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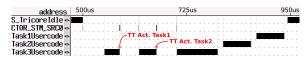
6.4 SLOTH ON TIME: Time-Triggered Laziness



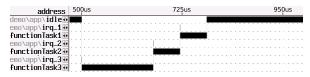
6 The SLOTH Approach | 6.4 SLOTH ON TIME: Time-Triggered Laziness

Qualitative Evaluation: AUTOSAR

Commercial AUTOSAR: **Priority inversion** with time-triggered activation (2,075 cycles each)



SLOTH ON TIME: avoids this by design!



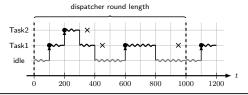
66 Interrupts are perhaps the biggest cause of priority inversion in real-time systems, causing the system to not meet all of its timing requirements. ??

> Stewart 1999: "Twenty-Five Most Common Mistakes with Real-Time Software Development" [12]

■ Idea: use hardware timer arrays to implement schedule tables

SLOTH ON TIME: Time-Triggered Laziness

- TC1796 GPTA: 256 timer cells, routable to 96 interrupt sources
 - use for task activation, deadline monitoring, execution time budgeting, time synchronization, and schedule table control
- SLOTH ON TIME implements OSEKtime [10] and AUTOSAR OS schedule tables [1]
 - combinable with Sloth or Sleepy Sloth for mixed-mode systems
 - up to 170x lower latencies compared to commercial implementations





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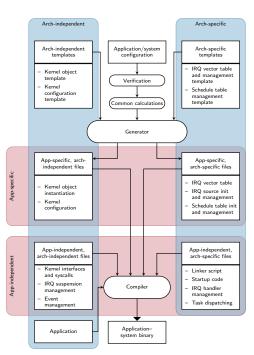
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- 6.5 **SLOTH**∗ Generation

SLOTH* Generation

- Two generation dimensions
 - Architecture
 - Application
- Generator is implemented in Perl
 - Templates
 - Configuration

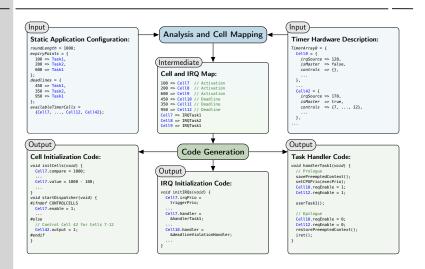




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- 6.1 Motivation: OSEK and Co
- 6.2 SLOTH: Threads as Interrupts
- 6.3 **SLEEPY SLOTH**: Threads as IRQs as Threads
- 6.4 SLOTH ON TIME: Time-Triggered Laziness
- 6.5 SLOTH* Generation
- 6.6 Summary and Conclusions
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SLOTH ON TIME Generation





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6 The SLOTH Approach | 6.5 SLOTH* Generation

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Summary: The SLOTH* Approach

- Exploit standard interrupt/timer hardware to delegate core OS functionality to hardware
 - scheduling and dispatching of control flows
 - OS needs to be tailored to application *and* hardware platform
 - \sim generative approach is necessary
- Benefits
 - tremendous latency reductions, very low memory footprints
 - unified control flow abstraction
 - hardware/software-triggered, blocking/run-to-completion
 - no need to distinguish between tasks and ISRs
 - no rate-monotonic priority inversion
 - reduces complexity
 - less work for the OS developer :-)







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6 The SLOTH Approach | 6.7 References

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