Konfigurierbare Systemsoftware (KSS)

VL 6 – Generative Programming: The SLOTH Approach

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About this Lecture

Problem Space

Solution Space

Features and Dependencies

Architecture and Implementation

Domain Expert

System User

intentional side

extensional side

Specific Problem

Specific Solution

Variant
Implementation Techniques: Classification

Decompositional Approaches
- Text-based filtering (untyped)
- Preprocessors

Compositional Approaches
- Language-based composition mechanisms (typed)
- OOP, AOP, Templates

Generative Approaches
- Metamodel-based generation of components (typed)
- MDD, C++ TMP, generators
Implementation Techniques: Classification

- Decompositional Approaches
  - Text-based filtering (untyped)
  - Preprocessors

- Compositional Approaches
  - Language-based composition mechanisms (typed)
    - OOP, AOP, Templates

- Generative Approaches
  - Metamodel-based generation of components (typed)
  - MDD, C++ TMP, generators

“I’d rather write programs to write programs than write programs.”

Dick Sites (DEC)
6.1 Motivation: OSEK and Co
6.2 SLOTH: Threads as Interrupts
6.3 SLEEPY SLOTH: Threads as IRQs as Threads
6.4 SAFER SLOTH: Hardware-Tailored Isolation
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   OSEK OS: Tailoring and Generation
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The OSEK Family of Automotive OS Standards

1995  OSEK OS (OSEK/VDX)  [9]
2001  OSEKtime (OSEK/VDX)  [11]
2005  AUTOSAR OS (AUTOSAR)  [1]

OSEK OS

- **statically configured**, event-triggered real-time OS

OSEKtime

- **statically configured**, time-triggered real-time OS
- can optionally be extended with OSEK OS (to run in slack time)

AUTOSAR OS

- **statically configured**, event-triggered real-time OS
- real superset of OSEK OS  
- backwards compatible
- additional time-triggered abstractions (schedule tables, timing protection)
- intended as a successor for both OSEK OS and OSEKtime
OSEK OS: Abstractions [9]

Control flows

- **Task**: software-triggered control flow (strictly priority-based scheduling)
  - Basic Task (BT) run-to-completion task with strictly stack-based activation and termination
  - Extended Task (ET) may suspend and resume execution ($\leftrightarrow$ coroutine)

- **ISR**: hardware-triggered control flow (hardware-defined scheduling)
  - Cat 1 ISR (ISR1) runs below the kernel, may not invoke system services ($\leftrightarrow$ prologue without epilogue)
  - Cat 2 ISR (ISR2) synchronized with kernel, may invoke system services ($\leftrightarrow$ epilogue without prologue)

- **Hook**: OS-triggered signal/exception handler
  - ErrorHook invoked in case of a syscall error
  - StartupHook invoked at system boot time
  - ...
Coordination and synchronization

- **Resource**: mutual exclusion between well-defined set of tasks
  - stack-based priority ceiling protocol ([12]):
    - `GetResource()` → priority is raised to that of highest participating task
  - pre-defined `RES_SCHED` has highest priority (→ blocks preemption)
  - implementation-optional: task set may also include cat 2 ISRs

- **Event**: condition variable on which ETs may block
  - part of a task’s context

- **Alarm**: asynchronous trigger by HW/SW counter
  - may execute a callback, activate a task, or set an event on expiry
OSEK OS: System Services (Excerpt)

- **Task-related services**
  - **ActivateTask(task)** → task is active (leadsto ready), counted
  - **TerminateTask()** → running task is terminated
  - **Schedule()** → active task with highest priority is running
  - **ChainTask(task)** → atomic

- **Resource-related services**
  - **GetResource(res)** → current task has res ceiling priority
  - **ReleaseResource(res)** → current task has previous priority

- **Event-related services (extended tasks only!)**
  - **SetEvent(task, mask)** → events in mask for task are set
  - **ClearEvent(mask)** → events in mask for current task are unset
  - **WaitEvent(mask)** → current task blocks until event from mask has been set

- **Alarm-related services**
  - **SetAbsAlarm(alarm, ...)** → arms alarm with absolute offset
  - **SetRelAlarm(alarm, ...)** → arms alarm with relative offset
OSEK OS: Conformance Classes [9]

OSEK offers predefined tailorability by four **conformance classes**

- **BCC1** only basic tasks, limited to one activation request per task and one task per priority, while all tasks have different priorities
- **BCC2** like BCC1, plus more than one task per priority possible and multiple requesting of task activation allowed
- **ECC1** like BCC1, plus extended tasks
- **ECC2** like ECC1, plus more than one task per priority possible and multiple requesting of task activation allowed for basic tasks

The OSEK feature diagram
An OSEK OS instance is configured \textbf{completely statically}

- all general OS features (hooks, ...)
- all instances of OS abstractions (tasks, ...)
- all relationships between OS abstractions
described in a domain-specific language (DSL)

OIL: The \textbf{OSEK Implementation Language}

- standard types and attributes (\texttt{TASK}, \texttt{ISR}, ...)
- vendor/plattform-specific \textit{attributes}
  (ISR source, priority, triggering)
- task types and conformance class is deduced

\begin{verbatim}
OSEK OS: System Specification with OIL [10]

\begin{small}

OIL File for Example System (BCC1)

- Three basic tasks: Task1, Task3, Task4
- Category 2 ISR: ISR2 (platform-spec. source/priority)
- Task1 and Task3 use resource Res1 \leadsto ceiling pri = 3
- Alarm Alarm1 triggers Task4 on expiry

\end{small}
\end{verbatim}
OSEK OS: System Generation [10, p. 5]

- User's source code
  - C code

- System Generator (SG)
  - Application configuration files (OIL)
  - Files produced by SG

- Compiler
- Linker
- Executable file

- OSEK Builder
  - OSEK components, tools & related files
  - User written/defined
  - Third party tools & related files

- Make tool
Basic tasks behave much like IRQ handlers (on a system with support for IRQ priority levels)
- priority-based dispatching with run-to-completion
- LIFO, all control flows can be executed on a single shared stack

So why not dispatch tasks as ISRs?

 proposé: Let the hardware do all scheduling!

proposé: Let’s be a SLOTH!
6.1 Motivation: OSEK and Co

6.2 **SLOTH**: Threads as Interrupts
   - Basic Idea
   - Design
   - Results
   - Limitation

6.3 **SLEEPY SLOTH**: Threads as IRQs as Threads

6.4 **SAFER SLOTH**: Hardware-Tailored Isolation

6.5 **SLOTH ON TIME**: Time-Triggered Laziness

6.6 **SLOTH\* Generation**

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Idea: threads are interrupt handlers, synchronous thread activation is IRQ

Let interrupt subsystem do the scheduling and dispatching work

Applicable to priority-based real-time systems

Advantage: small, fast kernel with unified control-flow abstraction
IRQ system must support priorities and software triggering
SLOTH: Example Control-Flow

CPU Prio Level

0 1 2 3 4

init()

enable()

Task1

GetRes(Res1)

ISR2

RelRes(Res1)

SetAlarm(Al1)

iret

Task1

Term()

idle()

Alarm1

Task4

Term()

Task1

Act(Task1)

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SLOTH: Qualitative Results

- Concise kernel design and implementation
  - < 200 LoC, < 700 bytes code memory, very little RAM

- Single control-flow abstraction for tasks, ISRs (1/2), callbacks
  - Handling oblivious to how it was triggered (by hardware or software)

- Unified priority space for tasks and ISRs
  - No rate-monotonic priority inversion [3, 4]

- Straight-forward synchronization by altering CPU priority
  - Resources with ceiling priority (also for ISRs!)
  - Non-preemptive sections with RES_SCHEDULER (highest task priority)
  - Kernel synchronization with highest task/cat.-2-ISR priority
Performance Evaluation: Methodology

- Reference implementation for Infineon TriCore
  - 32-bit load/store architecture
  - Interrupt controller: 256 priority levels, about 200 IRQ sources with memory-mapped registers
  - Meanwhile also implementations for ARM Cortex-M3 (SAM3U) and x86

- Evaluation of task-related system calls:
  - Task activation
  - Task termination
  - Task acquiring/releasing resource

- Comparison with commercial OSEK implementation and CiAO

- Two numbers for SLOTH: best case, worst case
  - Depending on number of tasks and system frequency
Performance Evaluation: Results

- Activate(): \( \approx 2x \) w/ dispatch
- Activate(): \( \approx 4x \) w/ dispatch
- Terminate(): \( \approx 20x \)
- Chain(): \( \approx 5x \)
- GetRes(): \( \approx 3x \)
- ReleaseRes(): \( \approx 8x \)
- ReleaseRes(): \( \approx 8x \)

Cycles

- Speed-Up
  - CiAO
  - Commercial OSEK

- SLOTH best case
- SLOTH worst case
- CiAO
- Commercial OSEK
Limitations of the SLOTH Approach

- No multiple tasks per priority (OSEK BCC2 / ECC2) → execution order has to be the same as activation order
- No extended tasks (that is, events, OSEK ECC1 / ECC2) → impossible with stack-based IRQ execution model
- No safety (that is, AUTOSAR-OS memory protection) → impossible if everything runs as IRQ handler
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<table>
<thead>
<tr>
<th></th>
<th>Activation Event</th>
<th>Sched./Disp.</th>
<th>Semantics</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISRs</td>
<td>HW</td>
<td>by HW</td>
<td>RTC</td>
</tr>
<tr>
<td>Threads</td>
<td>SW</td>
<td>by OS</td>
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</tr>
<tr>
<td>SLOTH [6]</td>
<td>HW or SW</td>
<td>by HW</td>
<td>RTC</td>
</tr>
<tr>
<td>SLEEPY SLOTH [7]</td>
<td>HW or SW</td>
<td>by HW</td>
<td>RTC or Blocking</td>
</tr>
</tbody>
</table>

(RTC: Run-to-Completion)
Main Goal
Support extended blocking tasks (with stacks of their own), while preserving SLOTH’s latency benefits by having threads run as ISRs.

Main Challenge
IRQ controllers do not support suspension and re-activation of ISRs.
**SLEEPY SLOTH Design: Task Prologues and Stacks**

- **Hardware Periphery**
  - HW IRQ
  - Alarm Exp.

- **Timer System**
  - Alarm Exp.

- **IRQ Sources**
  - **ExtTask1**
    - prio=1
    - req
    - IE
  - **ISR2**
    - prio=2
    - request
  - **Task3**
    - prio=3
    - request
  - **ExtTask4**
    - prio=4
    - req
    - IE

- **IRQ Arbitration Unit**
  - CPU
    - curprio=X

- **IRQ Vector Table**
  - prol1()
  - task1()
  - isr2()
  - prol3()
  - task3()
  - prol4()
  - task4()

- **Task Stack**
  - Stack ET1
  - Stack ET4
**SLEEPY SLOTH: Dispatching and Rescheduling**

- Task prologue: switch stacks if necessary
  - Switch *basic task* → *basic task* omits stack switch
  - On job start: initialize stack
  - On job resume: restore stack

- Task termination: task with next-highest priority needs to run
  - Yield CPU by setting priority to zero
  - (Prologue of *next* task performs the stack switch)

- Task blocking: take task out of “ready list”
  - Disable task’s IRQ source
  - Yield CPU by setting priority to zero

- Task unblocking: put task back into “ready list”
  - Re-enable task’s IRQ source
  - Re-trigger task’s IRQ source by setting its pending bit
**SLEEPY SLOTH: Example Control Flow**

**Diagram Description:**

- **CPU/Task Priority:**
  - Task BT1
  - Task ET3
  - Task BT2

- **Prologue ET3**
  - Task ET3
  - Prologue ET3
  - save(stk_bt)
  - load(stk_et3)
  - Task ET3 (ctd.)

- **Prologue BT1**
  - Task BT1
  - Prologue BT1
  - save(stk_et3)
  - load(stk_bt)
  - Task BT1 (ctd.)

- **Prologue BT2**
  - Task BT2
  - Prologue BT2
  - nop
  - Prologue ET3 Task ET3 (ctd.)

- **Unblock(ET3)**
  - Task ET3
  - Unblock(ET3)
  - save(stk_et3)
  - load(stk_et3)
  - Task ET3 (ctd.)

- **IRQ Source**
  - Task1
    - prio=1
    - request
  - Task2
    - prio=2
    - request
  - ExtTask3
    - prio=3
    - req

- **IRQ Arbitration Unit**
  - CPU
    - curprio=3
  - IRQ Vector Table
    - prol1() -> task1()
    - prol2() -> task2()
    - prol3() -> task3()

- **Basic Stack**
  - Stack ET3

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Evaluation: Extended and Basic Tasks

Basic switches in a mixed system only slightly slower than in purely basic system
Limitations of the SLOTH Approach

- No multiple tasks per priority (OSEK BCC2 / ECC2)
  - execution order has to be the same as activation order

- No extended tasks (that is, events, OSEK ECC1 / ECC2)
  - impossible with stack-based IRQ execution model

- No safety (that is, AUTOSAR-OS memory protection)
  - impossible if everything runs as IRQ handler
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Main Goal
Support isolation of state and privileges, while preserving SLOTH’s latency benefits by having threads run as ISRs.

Main Challenge
ISRs run in supervisor mode with full privileges. So how to
- Effectively isolate kernel and application
- Maintain design principles of Sloth
Memory Protection in Embedded Systems

- **Safety, but not security**
- **Protect the data, but not the code**
- Safety model based on AUTOSAR OS
- MPU-based isolation

**Vertically:** Protect kernel state and MPU configuration

**Horizontally:** Isolate applications or even tasks from each other
Maintaining the SLOTH Principles for SAFER SLOTH

- Exploit as much knowledge about target hardware as possible
- Tailor kernel to fit both the platform and the application
- Taking into account:
  - Extent and layout of MPU configuration
  - Method for re-programming the MPU
  - Available hardware privilege levels
  - Is MPU active in all levels?
  - Degree of safety required by the application
Protection Modes in *SAFER SLOTH*

**Unsafe**
- The original Sloth OS, without isolation

**MPU**
- MPU active, but tasks execute with supervisor privileges
- Vertical isolation ensured constructively in post-validation

**MPU+traps**
- Vertical isolation ensured by hardware privilege levels
- System services acquire kernel privileges via syscall mechanism
SAFER SLOTH: Architecture

**Static Configuration**

System Configuration:
- Protection mode: unsafe
- Application Configuration:
  - Tasks: Task1, Task2, Task3
  - Domains: Dom1, Dom2, Dom3
  - Data: var1, var2, var3, var4

**Hardware Model**

TriCore TC1796:
- MPU ranges: 4
- MPU range sets: 2
- Privilege levels: 3
  - 0 = user mode
  - 1 = user mode with periphery access
  - 2 = supervisor mode
- MPU active in supervisor mode: ✓
- Post-validation available: ✓

**Task → MPU Ranges Map**

Syntax: \([\text{range idx}] = \{\text{from}, \text{to}\}\)

**Task1 MPU Ranges:**
- [0] = \{BEGIN_stack, %sp\}
- [1] = \{BEGIN_Dom1, END_Dom1\}

**Task2 MPU Ranges:**
- [0] = \{BEGIN_stack, %sp\}
- [1] = \{BEGIN_Dom2, END_Dom2\}

**Task3 MPU Ranges:**
- [0] = \{BEGIN_stack, %sp\}
- [1] = \{BEGIN_Dom3, END_Dom3\}

**Memory Map**

- Stack:
  - BEGIN_stack
  - END_stack
- Dom1:
  - var1
  - END_Dom1
- Dom2:
  - var2
  - BEGIN_Dom2
- Dom3:
  - var3
  - var4
  - etc.
MPU mode in Safer SLOTH

Unsafe Mode:

Task1:
...
; inlined call to GetResource(Res1):
  prio = getCurPrio();
  pushResourceStack(prio);
  if (Res1 > prio) {
    setCurPrio(Res1);
  }
...

MPU Mode:

Task1:
...
; disable MPU
  mfcr %d15,$psw
  insert %d15,%d15,0,12,1
  mtcr $psw,%d15
  prio = getCurPrio();
  pushResourceStack(prio);
  if (Res1 > prio) {
    setCurPrio(Res1);
  }
; enable MPU
  mfcr %d15,$psw
  insert %d15,%d15,15,12,1
  mtcr $psw,%d15
...

User mode

Supervisor mode

System service implementation
MPU+traps mode in SAFER SLOTH

MPU+traps Mode:

Task1:
...
syscall 2
...

trap_6: ; syscall trap
<syscall dispatcher>
ji ...

real_GetResource:
prio = getCurPrio();
pushResourceStack(prio);
<...>
<non-inlined implementation>
<...>

rfe

Supervisor mode
System service implementation
User mode
The Problem with Traps

- **SLOTH** gains a lot of its benefits through compiler optimizations
  - Inlining of system service calls
  - Removal of dead code
  - Constant propagation

- Traditional traps **prohibit** such optimizations
  - System services must be standalone functions
  - Jumped to via a syscall dispatcher

**Solution Idea**

*Combine* MPU and MPU+traps mode

\[ \leadsto \text{Inline \textit{traps} as 4th protection mode (MPU+itraps)} \]
Inline Traps in SAFER SLOTH

MPU+itraps Mode:

Task1:
...  
**syscall** 0
prio = getCurPrio();  
pushResourceStack(prio);
if (Res1 > prio) {
    setCurPrio(Res1);
}

; load current pc
mfcr %d15,$pc
add  %d15,2
; overwrite return address
mov.a %a11,%d15
rfe...

returns to

generates trap
jumps back

; syscall trap
trap_6:

ji %a11

User mode

Supervisor mode

System service implementation

System service implementation
Evaluation Results: Total Overheads

Safer Sloth vs. commercial AUTOSAR OS

Safer Sloth (unsafe mode)
△ MPU / +traps / +itraps
AUTOSAR OS (unsafe)

Cycles

Activate w/o disp.
Activate w/ disp.
Terminate w/ disp.
ChainTask w/ disp.
GetResource w/o disp.
ReleaseRes w/o disp.
ReleaseRes w/ disp.
Safer Sloth vs. commercial AUTOSAR OS

Evaluation Results: Additional Overheads

- Safer Sloth (unsafe mode)
- \(\Delta\) MPU / +traps / +itraps
- AUTOSAR OS (\(\Delta\) MPU+traps)

**Cycles**

- Activate w/o disp.
- Activate w/ disp.
- Terminate w/ disp.
- ChainTask w/ disp.
- GetResource w/o disp.
- ReleaseRes w/o disp.
- ReleaseRes w/ disp.

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**SLOTH ON TIME: Time-Triggered Laziness**

- **Idea:** use hardware timer arrays to implement schedule tables

- **TC1796 GPTA:** 256 timer cells, routable to 96 interrupt sources
  - use for task activation, deadline monitoring, execution time budgeting, time synchronization, and schedule table control

- **SLOTH ON TIME** implements OSEKtime [11] and AUTOSAR OS schedule tables [1]
  - combinable with SLOTH or SLEEPY SLOTH for mixed-mode systems
  - up to 170x lower latencies compared to commercial implementations
Qualitative Evaluation: AUTOSAR

Commercial AUTOSAR: **Priority inversion** with time-triggered activation (2,075 cycles each)

*Sloth on Time*: avoids this *by design!*

“Interrupts are perhaps the biggest cause of priority inversion in real-time systems, causing the system to not meet all of its timing requirements.”

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**SLOTH** Generation

- Two generation dimensions
  - Architecture
  - Application

Generator is implemented in Perl
- Templates
- Configuration
SLOTH ON TIME Generation

Input

Static Application Configuration:

\[\text{roundLength} = 1000;\]
\[\text{expiryPoints} = \{\]
\[100 \Rightarrow \text{Task1},\]
\[200 \Rightarrow \text{Task2},\]
\[600 \Rightarrow \text{Task1}\};\]
\[\text{deadlines} = \{\]
\[450 \Rightarrow \text{Task1},\]
\[350 \Rightarrow \text{Task2},\]
\[950 \Rightarrow \text{Task1}\};\]
\[\text{availableTimerCells} = \{\text{Cell7}, \ldots, \text{Cell12, Cell42}\};\]

Analysis and Cell Mapping

Intermediate

Cell and IRQ Map:

\[100 \Rightarrow \text{Cell7} // Activation\]
\[200 \Rightarrow \text{Cell8} // Activation\]
\[600 \Rightarrow \text{Cell10} // Activation\]
\[450 \Rightarrow \text{Cell10} // Deadline\]
\[350 \Rightarrow \text{Cell11} // Deadline\]
\[950 \Rightarrow \text{Cell12} // Deadline\]
\[\text{Cell7} \Rightarrow \text{IRQTask1}\]
\[\text{Cell8} \Rightarrow \text{IRQTask2}\]
\[\text{Cell9} \Rightarrow \text{IRQTask1}\]

Code Generation

Output

Cell Initialization Code:

\[\text{void initCells(}\text{void}\text{)}\{\]
\[\text{Cell7.compare} = 1000;\]
\[\text{...}\]
\[\text{Cell7.value} = 1000 - 100;\]
\[\text{...}\]
\[\text{void startDispatcher(}\text{void}\text{)}\{\]
\[\text{#ifndef CONTROLCELLS}\]
\[\text{Cell7.enable} = 1;\]
\[\text{...}\]
\[\text{#else}\]
\[\text{// Control Cell 42 for Cells 7-12}\]
\[\text{Cell42.output} = 1;\]
\[\text{#endif}\]
\[\text{}\}\

Input

Timer Hardware Description:

\[\text{TimerArray0} = \{\]
\[\text{Cell0} = \{\]
\[\text{irqSource} = 128,\]
\[\text{isMaster} = \text{false},\]
\[\text{controls} = \{\}\},\]
\[\text{...}\]
\[\text{Cell42} = \{\]
\[\text{irqSource} = 170,\]
\[\text{isMaster} = \text{true},\]
\[\text{controls} = \{7, \ldots, 12\},\]
\[\text{...}\]
\[\}\];\]

Output

Task Handler Code:

\[\text{void handlerTask1(}\text{void}\text{)}\{\]
\[\text{// Prologue}\]
\[\text{savePreemptedContext();}\]
\[\text{setCPUPrio(execPrio);}\]
\[\text{Cell10.reqEnable} = 1;\]
\[\text{Cell12.reqEnable} = 1;\]
\[\text{userTask1();}\]
\[\text{// Epilogue}\]
\[\text{Cell10.reqEnable} = 0;\]
\[\text{Cell12.reqEnable} = 0;\]
\[\text{restorePreemptedContext();}\]
\[\text{iret();}\]
\[\}\]

Output

IRQ Initialization Code:

\[\text{void initIRQs(}\text{void}\text{)}\{\]
\[\text{Cell7.irqPrio} = \text{triggerPrio};\]
\[\text{...}\]
\[\text{Cell7.handler} = \&\text{handlerTask1};\]
\[\text{...}\]
\[\text{Cell10.handler} = \&\text{deadlineViolationHandler};\]
\[\text{...}\]
\[\}\]

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Summary: The SLOTH* Approach

- Exploit standard interrupt/timer/mpu hardware to delegate core OS functionality to hardware
  - scheduling and dispatching of control flows
  - OS needs to be tailored to application and hardware platform
    \[\leadsto\] generative approach is necessary

Benefits

- tremendous latency reductions, very low memory footprints
- unified control flow abstraction
  - hardware/software-triggered, blocking/run-to-completion
  - no need to distinguish between tasks and ISRs
  - no rate-monotonic priority inversion
  - reduces complexity
- less work for the OS developer :-)

We are sloth
Referenzen


