

Ein Kontrollflussüberwachungsdienst für KESO-Anwendungen

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Friedrich-Alexander-Universität
Erlangen-Nürnberg



Zuverlässigkeit

Zuverlässigkeit und Fehlertoleranz

Kontrollflussfehler

Datenfehler

Kontrollflussüberwachung

„We present a[n] [...] version [...] (ECCA) [...] targeted for the **detection of control flow-errors with low overhead and low detection latency** [...]“

- Alkhalifa et al.: *Design and Evaluation of System-Level Checks for On-Line Control Flow Error Detection*

Zuverlässigkeit

Zuverlässigkeit und Fehlertoleranz

Kontrollflussfehler

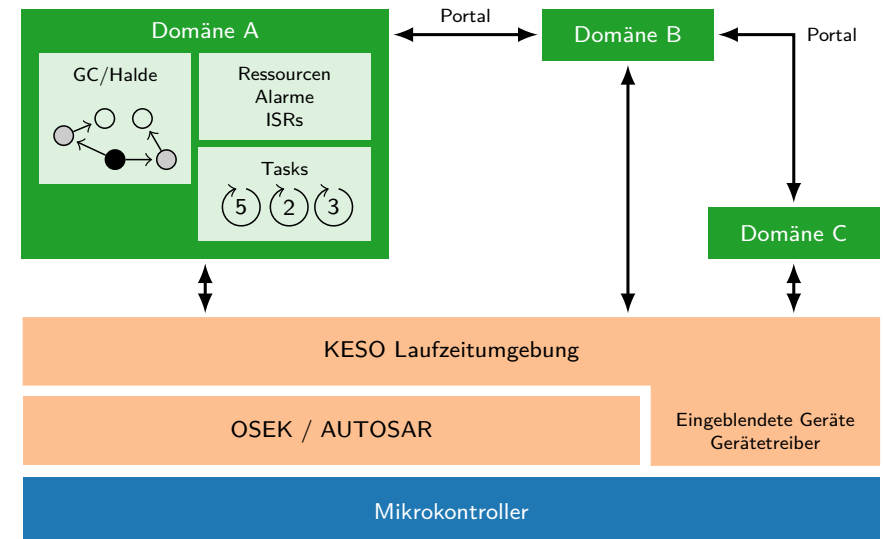
Datenfehler

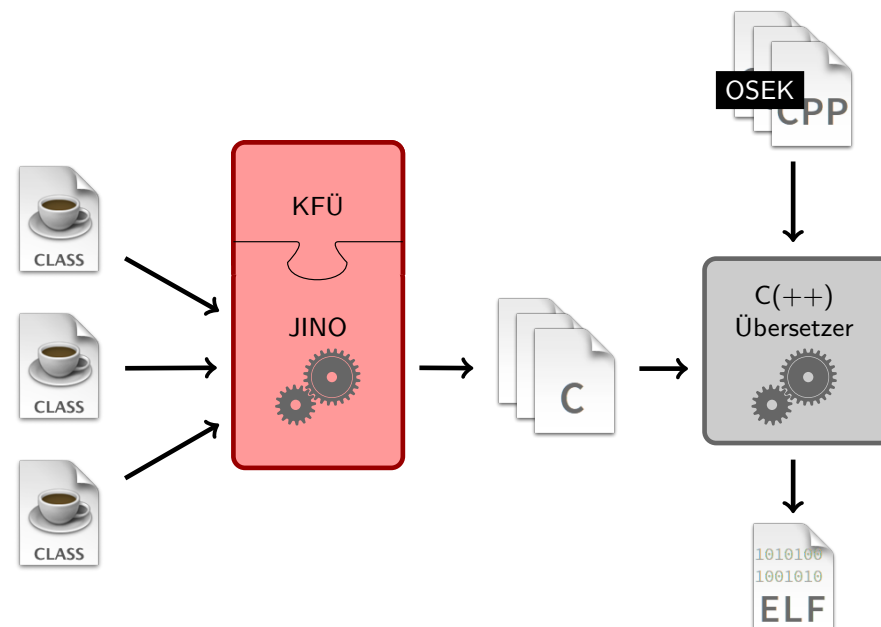
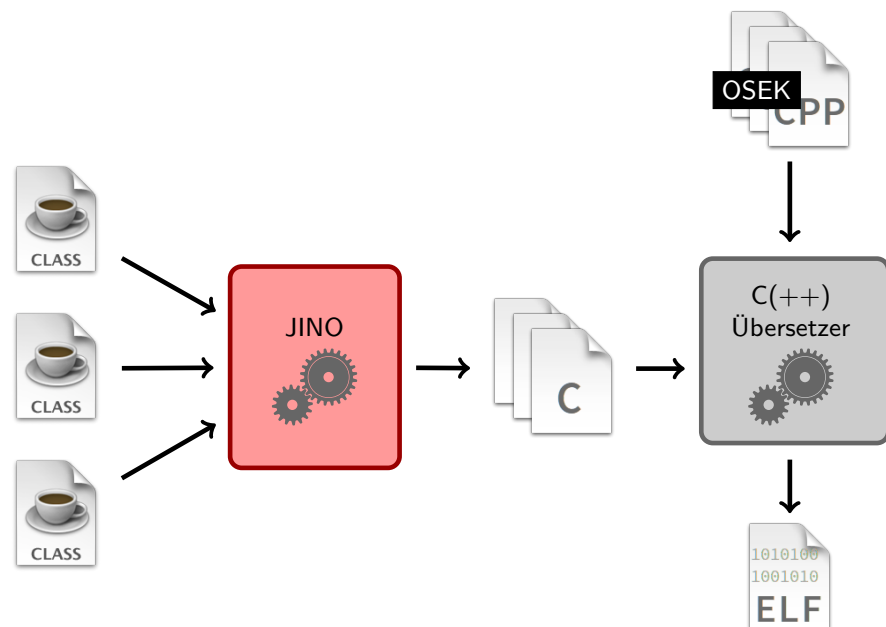
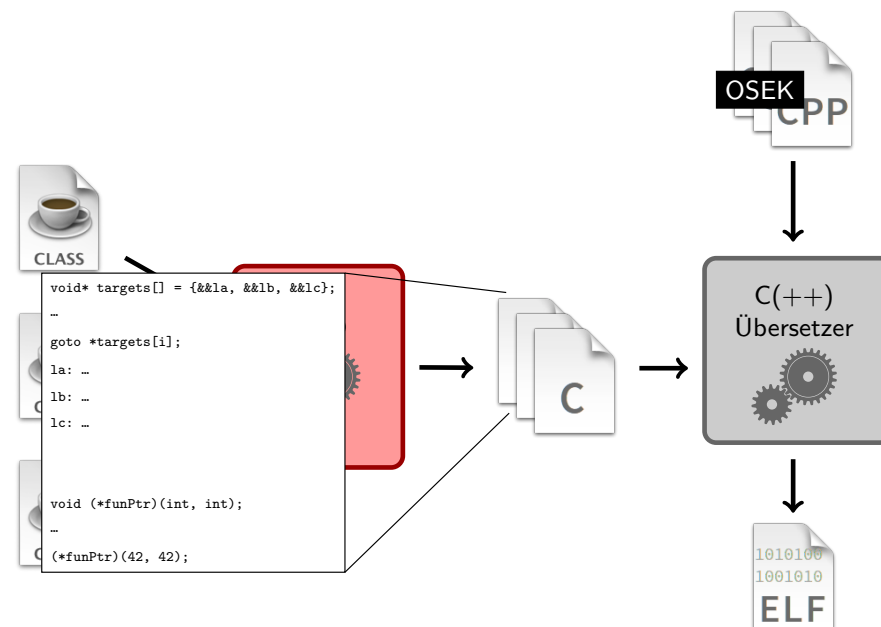
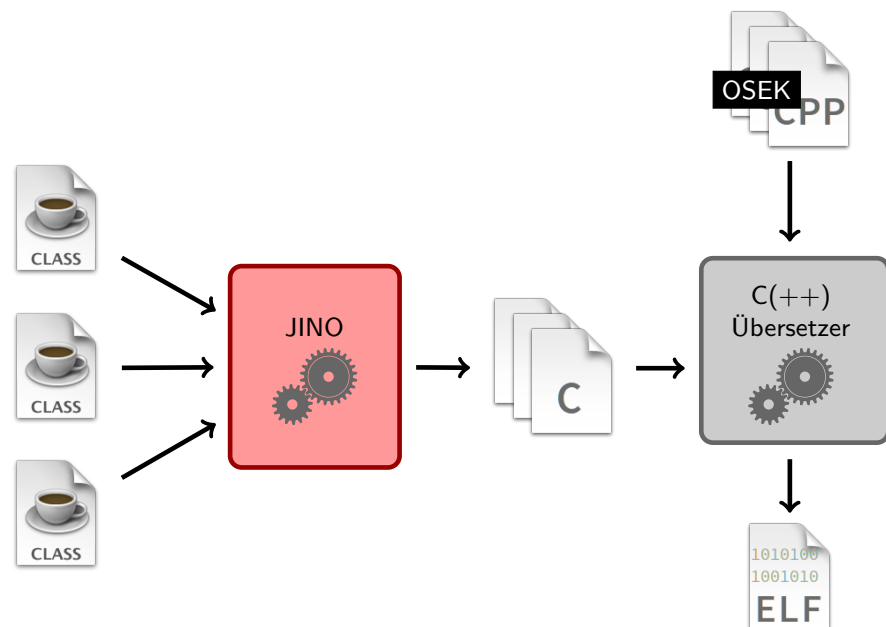
Kontrollflussüberwachung

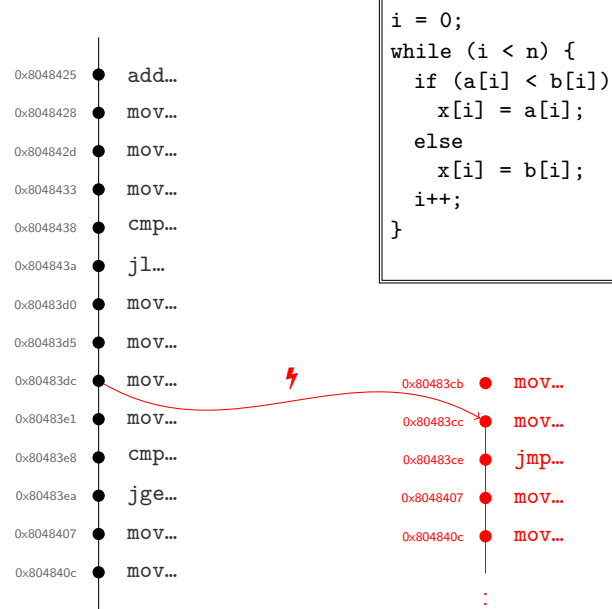
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KESO-Aufbau

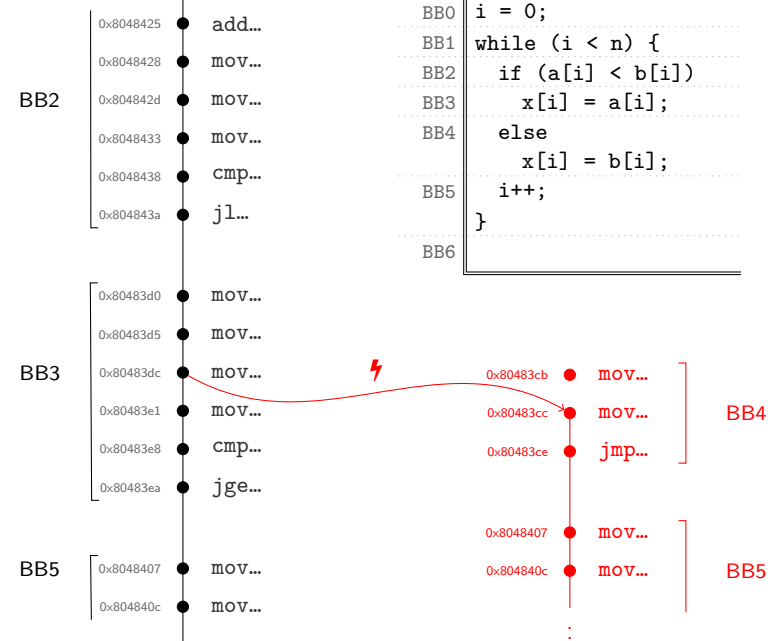






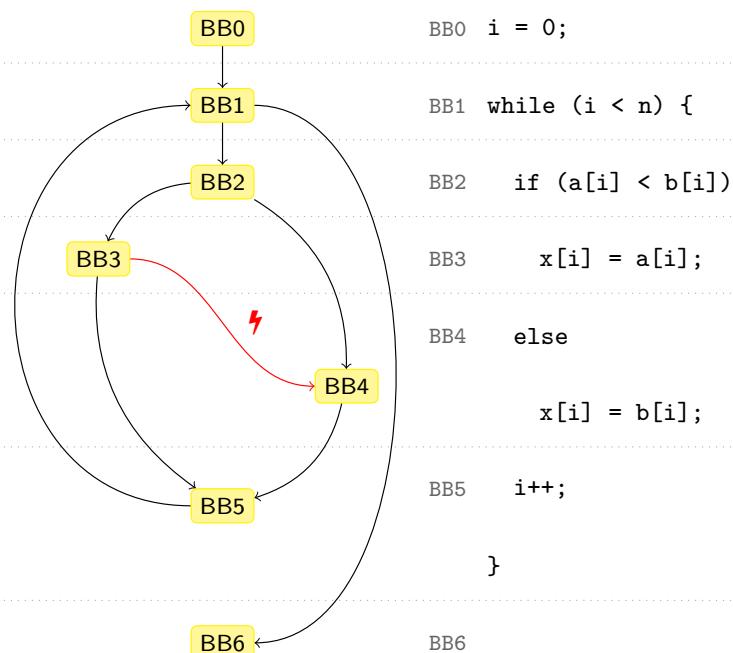
```
i = 0;
while (i < n) {
    if (a[i] < b[i])
        x[i] = a[i];
    else
        x[i] = b[i];
    i++;
}
```

```
0x80483cb mov...
0x80483cc mov...
0x80483ce jmp...
0x8048407 mov...
0x804840c mov...
...
```



```
BB0 i = 0;
BB1 while (i < n) {
BB2   if (a[i] < b[i])
BB3     x[i] = a[i];
BB4   else
BB5     x[i] = b[i];
BB6   i++;
}
```

```
0x80483cb mov...
0x80483cc mov...
0x80483ce jmp...
0x8048407 mov...
0x804840c mov...
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BB0 i = 0;
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Basisblockebene:

- Plain Interblock Error Detection [1], [2]
- Enhanced Control-Flow Checking using Assertions (ECCA) [3]
- Control-Flow Checking by Software Signatures (CFCSS) [4]
- Yet Another Control-Flow Checking using Assertions (YACCA) [5], [6]

Dominanzregionsebene:

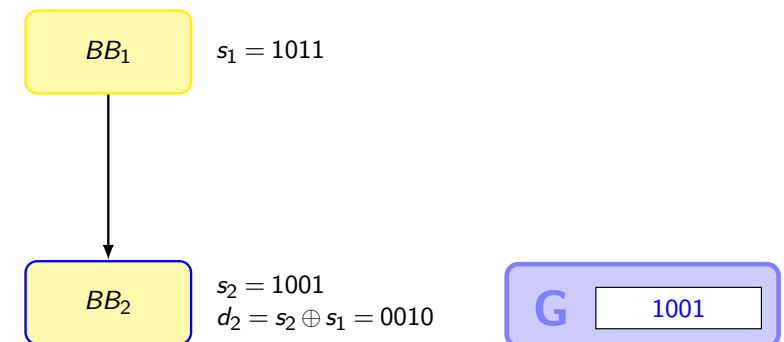
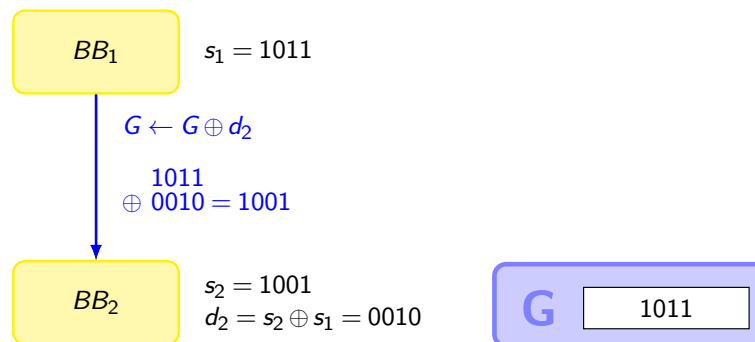
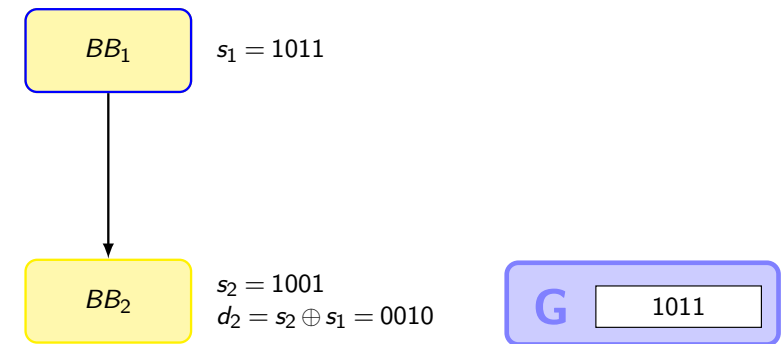
- Dominatorbasiertes Verfahren [7]
 - Vergabe-Strategien: „Kleinste“ und „Verteilung“
 - Schleifenoptimierung

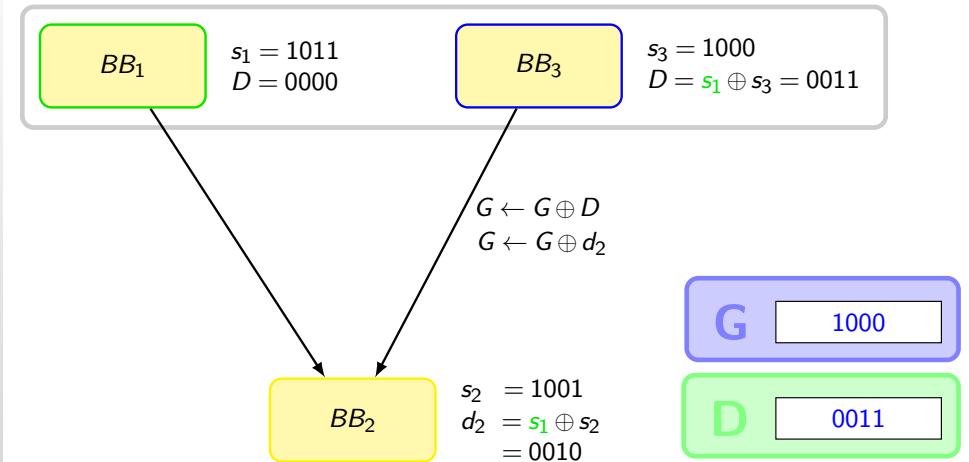
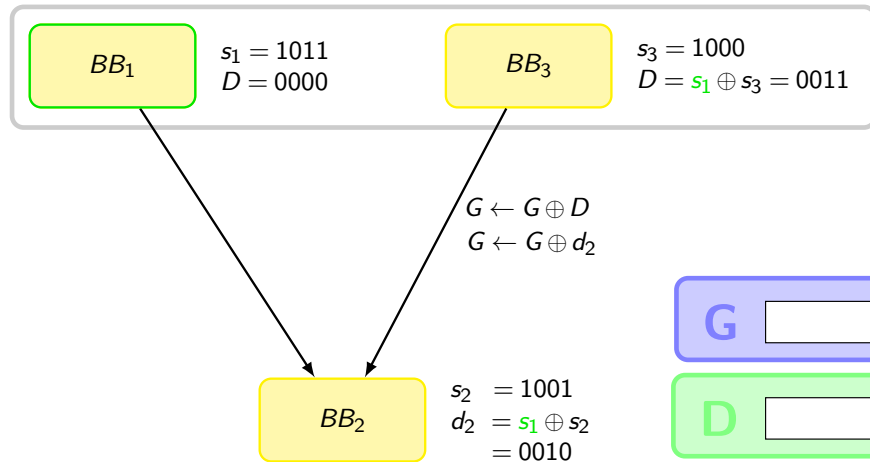
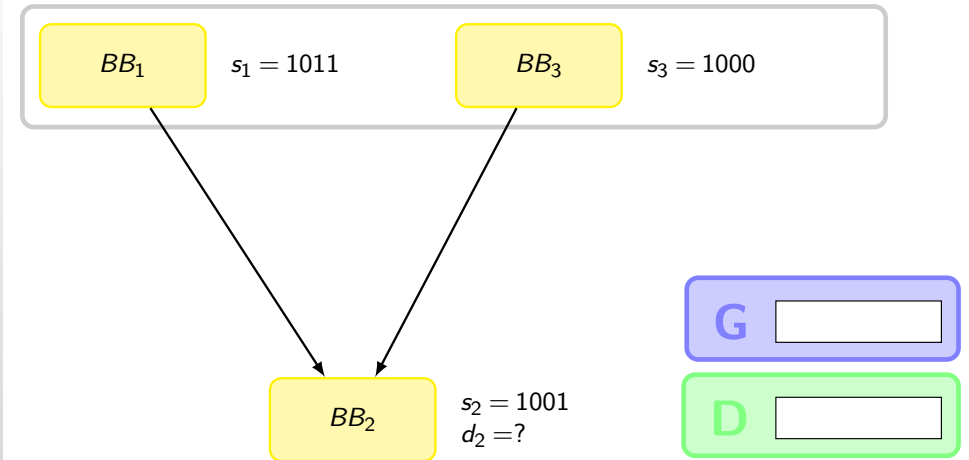
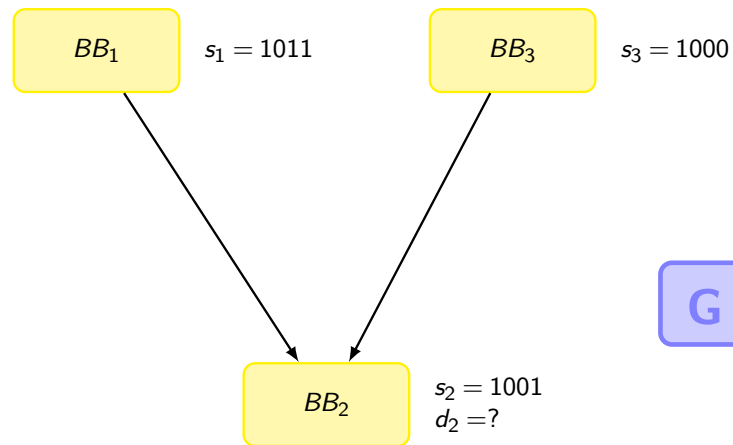
Basisblockebene:

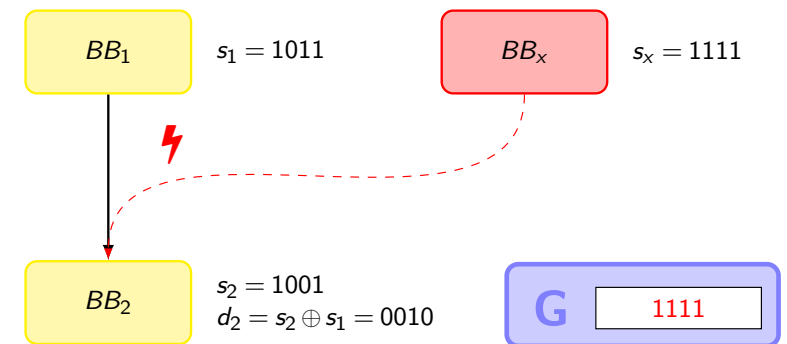
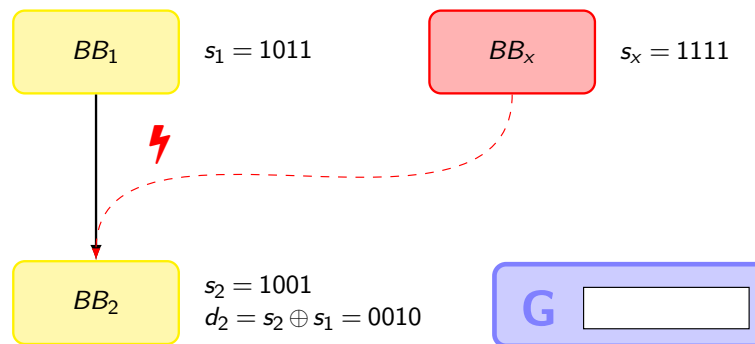
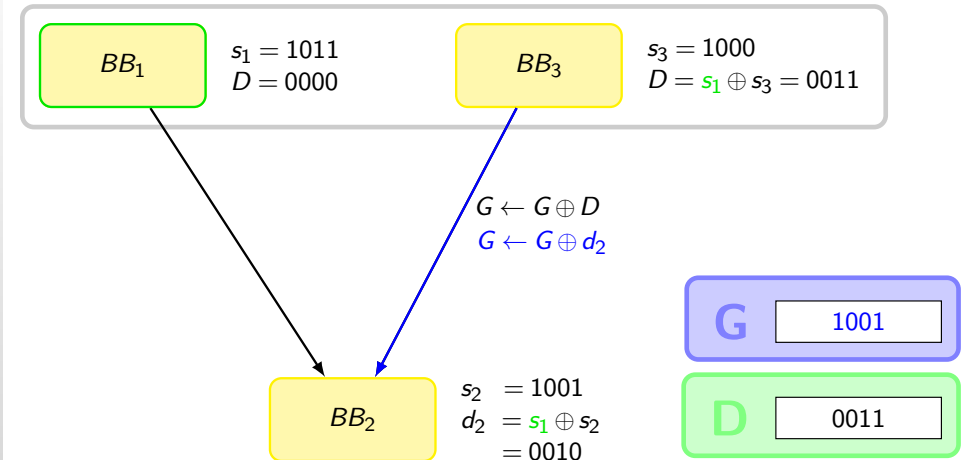
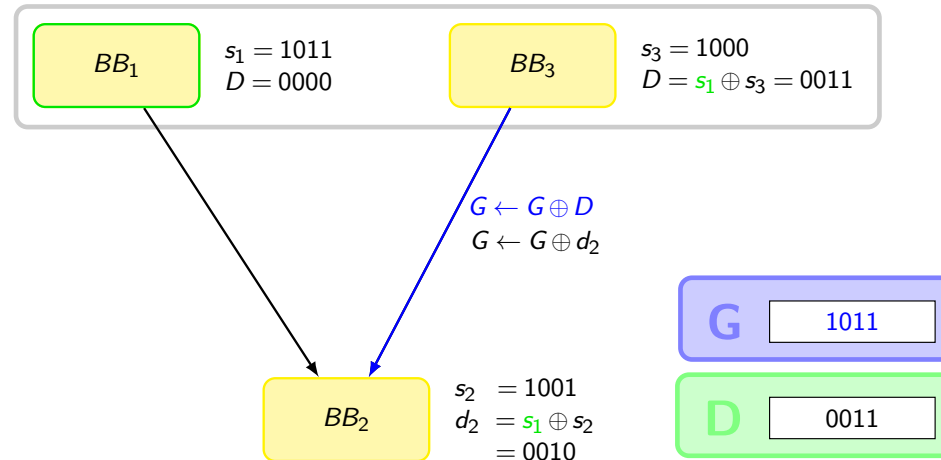
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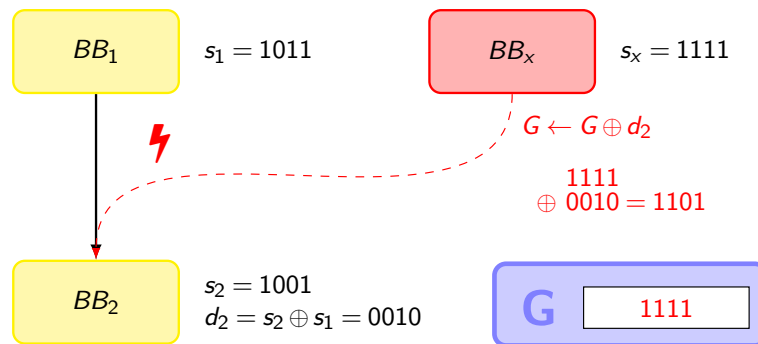
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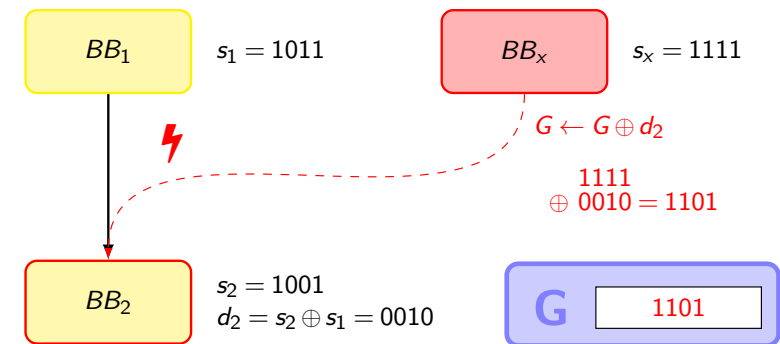
Umgesetzte Verfahren

Basisblockebene:

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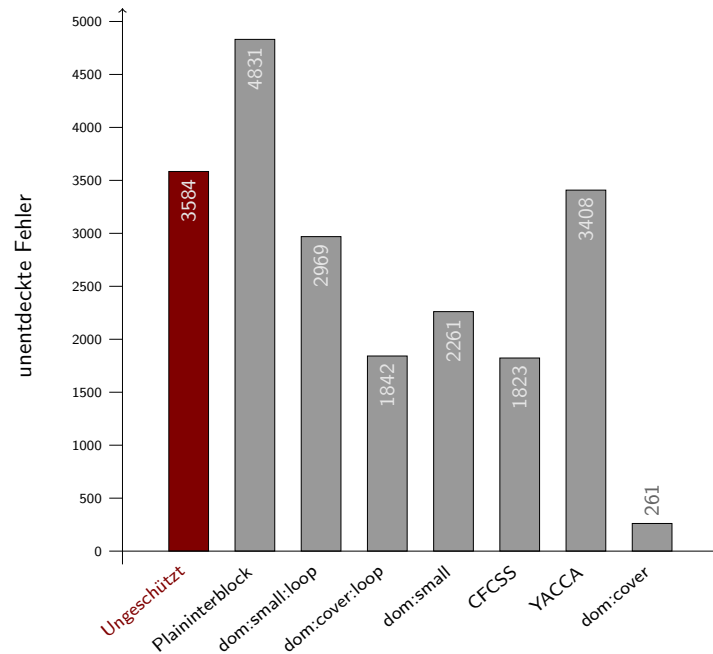
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Kontrollflussfehler



Unausgerichtete Sprünge

Ursprüngliche Instruktionsfolge	
0x1014af	83
0x1014b0	c2 add edx,0x1
0x1014b1	01
0x1014b2	0f
0x1014b3	af imul ecx,DWORD PTR
0x1014b4	4c [ebx+ebp*4+0x8]
0x1014b5	ab
0x1014b6	08
0x1014b7	01
0x1014b8	ce add esi,ecx
0x1014b9	0f
0x1014ba	b7 movzx ecx,WORD PTR
0x1014bb	48 [eax+0xa]
0x1014bc	0a
0x1014bd	83
0x1014be	f1 xor ecx,0x7
0x1014bf	07

Unausgerichtete Sprünge

Ursprüngliche Instruktionsfolge	Unausgerichtete Instruktionsfolge
0x1014af 83	
0x1014b0 c2 add edx,0x1	
0x1014b1 01	
0x1014b2 0f	
0x1014b3 af imul ecx,DWORD PTR	scas eax,DWORD PTR es:[edi]
0x1014b4 4c [ebx+ebp*4+0x8]	dec esp
0x1014b5 ab	stos DWORD PTR es:[edi],eax
0x1014b6 08	
0x1014b7 01	or BYTE PTR [ecx],al
0x1014b8 ce add esi,ecx	into
0x1014b9 0f	
0x1014ba b7 movzx ecx,WORD PTR	movzx ecx,WORD PTR
0x1014bb 48 [eax+0xa]	[eax+0xa]
0x1014bc 0a	
0x1014bd 83	
0x1014be f1 xor ecx,0x7	xor ecx,0x7
0x1014bf 07	

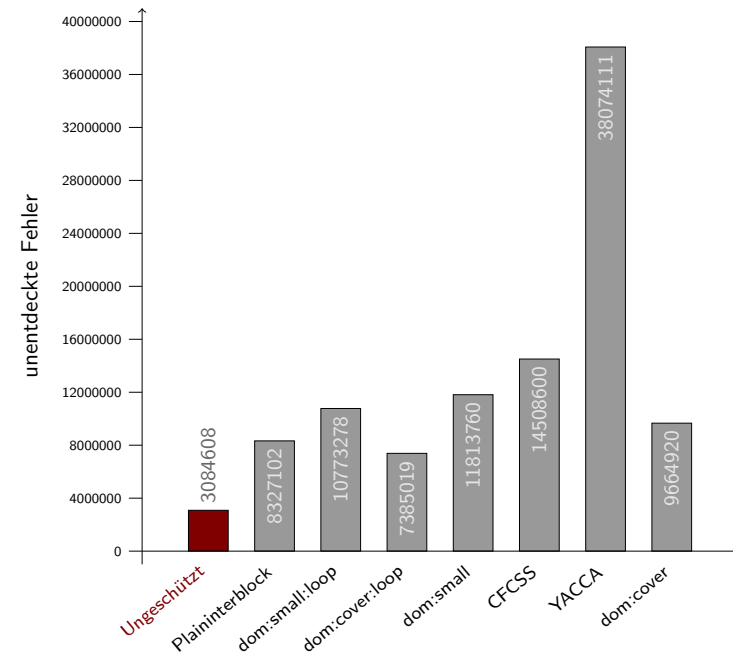
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0x1014b7 01	or BYTE PTR [ecx],al
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0x1014b9 0f	
0x1014ba b7 movzx ecx,WORD PTR	movzx ecx,WORD PTR
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0x1014bd 83	
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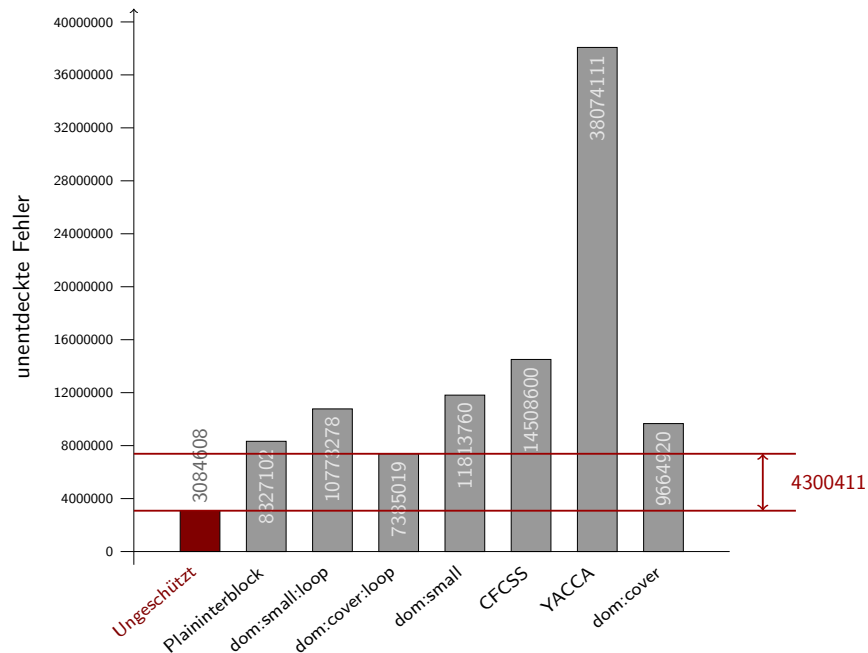
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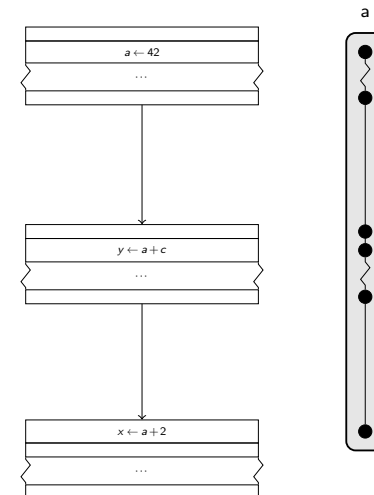
Allgemeine Einbitfehler

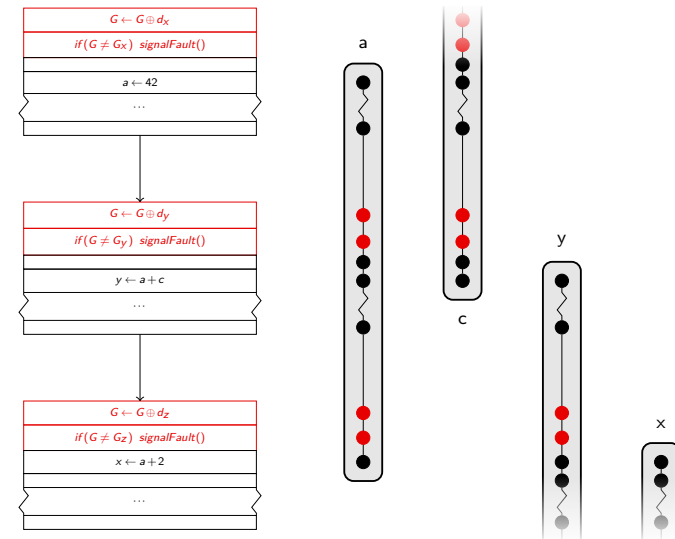
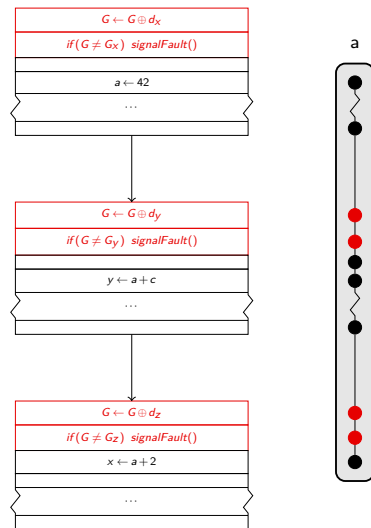


Allgemeine Einbitfehler

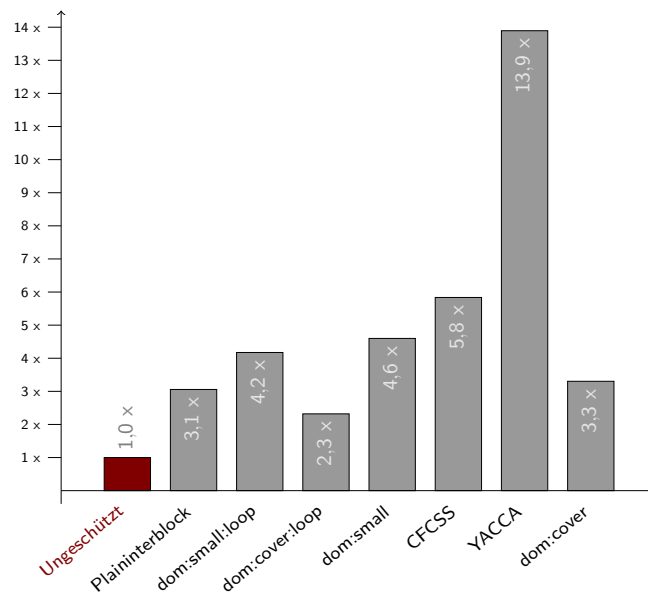


Datenfehler

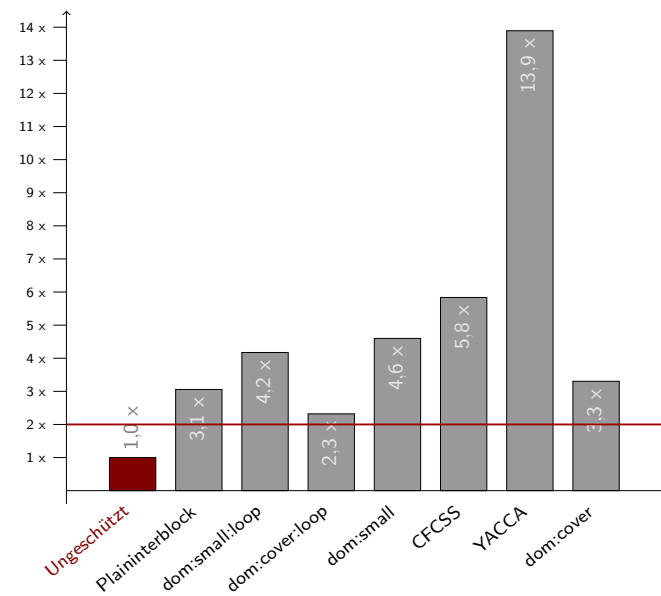




Laufzeit



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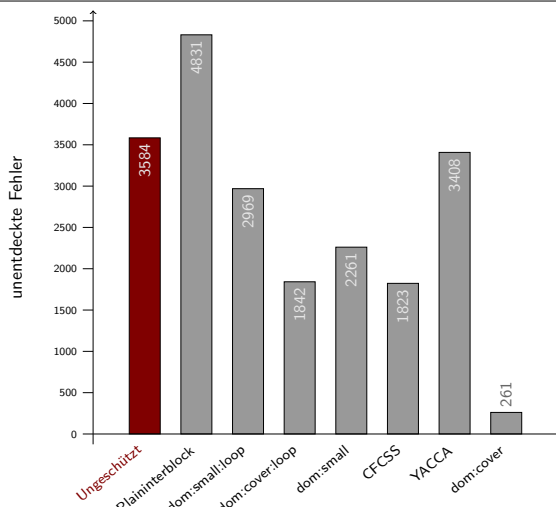


- 



Fazit

Kontrollflussfehler



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Fazit

Kontrollflussfehler

Unausgerichtete Sprünge

Ursprüngliche Instruktionsfolge	Unausgerichtete Instruktionsfolge
0x1014af 83 add edx,0x1	
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0x1014bb 48	
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0x1014bf 07	

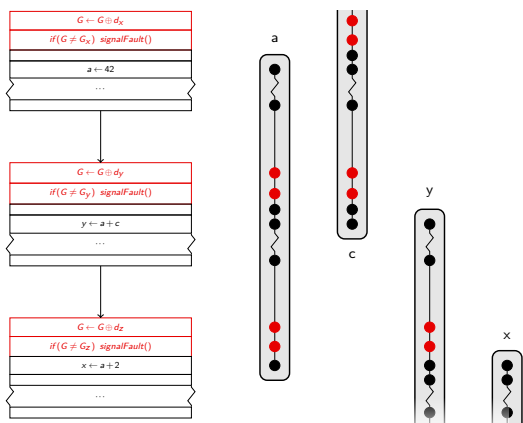
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Fazit

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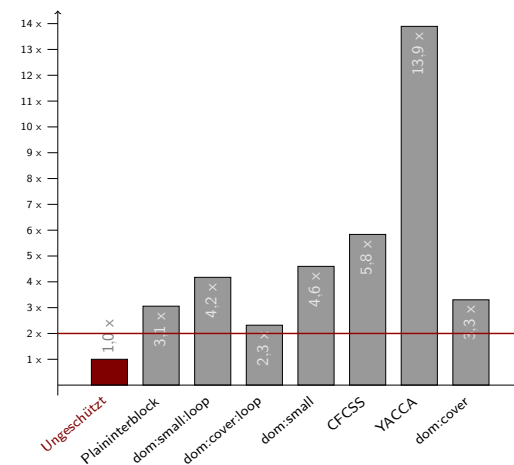
Fazit

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- [1] M. Rebaudengo, M. S. Reorda, M. Torchiano und M. Violante, „Soft-error detection through software fault-tolerance techniques,” in **Defect and Fault Tolerance in VLSI Systems, 1999. DFT’99. International Symposium on.** IEEE, 1999, S. 210–218.
- [2] P. Cheynet, B. Nicolescu, R. Velazco, M. Rebaudengo, M. Sonza Reorda und M. Violante, „Experimentally evaluating an automatic approach for generating safety-critical software with respect to transient errors,” **IEEE Transactions on Nuclear Science**, Vol. 47, Nr. 6, S. 2231–2236, 2000.
- [3] Z. Alkhalifa, V. S. Nair, N. Krishnamurthy und J. A. Abraham, „Design and evaluation of system-level checks for on-line control flow error detection,” **Parallel and Distributed Systems, IEEE Transactions on**, Vol. 10, Nr. 6, S. 627–641, 1999.
- [4] N. Oh, P. Shirvani und E. McCluskey, „Control-flow checking by software signatures,” **Reliability, IEEE Transactions on**, Vol. 51, Nr. 1, S. 111–122, Mar. 2002.
- [5] O. Goloubeva, M. Rebaudengo, M. S. Reorda und M. Violante, „Soft-error detection using control flow assertions,” in **Defect and Fault Tolerance in VLSI Systems, 2003. Proceedings. 18th IEEE International Symposium on.** IEEE, 2003, S. 581–588.
- [6] O. Goloubeva, M. Rebaudengo, M. Reorda und M. Violante, **Software-implemented hardware fault tolerance.** Springer, 2006.
- [7] C. Dietrich, „Global Optimization of Non Functional Properties in OSEK Real-Time Systems by Static Cross-Kernel Flow Analyses,” Masterarbeit, Universität Erlangen, Deutschland, Sep. 2014.

