Concurrent Systems

Nebenläufige Systeme

XIV. Pickings

Wolfgang Schröder-Preikschat

February 3, 2016
Agenda

Recapitulation
  Concurrent Systems

Perspectives
  Parallel Systems
  Computing Equipment
  Further Education
Outline

Recapitulation
Concurrent Systems

Perspectives
Parallel Systems
Computing Equipment
Further Education
Recapitulation
Concurrent Systems

Perspectives
Parallel Systems
Computing Equipment
Further Education
Main Research at the Chair

- **composability** and **configurability**
  - application-oriented (varying, type-safe) system software

- **specialisation**
  - dedicated operating systems: integrated, adaptive, parallel

- **reliability**
  - gentle fault and intrusion tolerance

- **thriftiness**
  - resource-aware operation of computing systems

- **timeliness**
  - migration paths between time- and event-triggered real-time systems

- **concurrency**
  - coordination of cooperation and competition between processes

“concurrent systems” is more or less **cross-cutting** thereto...
Latency Awareness in Operating Systems

- **latency prevention**
  - lock- and wait-free synchronisation
  - integrated generator-based approach

- **latency avoidance**
  - interference protection
  - race-conflict containment

- **latency hiding**
  - operating-system server cores
  - asynchronous remote system operation

- experiments with different **operating-system architectures**
  - process-/event-based and hardware-centric operating-system kernels
  - LAKE, Sloth

- DFG: 2 doctoral researchers, 2 student assistants

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\(^1\)http://univis.uni-erlangen.de → Research projects → LAOS
Coherency Kernel

- event-based minimal kernel
  - cache-aware main-memory footprint
  - hyper-threading of latent actions
- featherweight agreement protocols
  - overall kernel-level synchronisation
  - familie of consistency kernels
- problem-oriented consistency
  - sequential, entry, release consistency
  - functional hierarchy of consistency domains
  - memory domains for NUMA architectures
- implementation as to different processor architectures
  - partial or total, resp. {in,}coherent shared memory

DFG: 2 doctoral researchers (1 FAU, 1 BTU)

\(^2\)http://univis.uni-erlangen.de → Research projects → COKE
Heterogeneous Resource-Aware Multi-Processing

- **GPU-centric resource management**
  - timely predictable run-time system
    - run-to-completion kernel
  - prioritisation and isolation of GPU tasks
    - scheduling according to execution costs
  - trade-off handling as to throughput and response time

- **RAM-centric run-time executive** for heterogeneous processors
  - application-specific and problem-orientied memory management
  - run-time adaptation and relocation of dynamic data structures

- **tailor-made system software** for heterogeneous image systems
  - support of an incremental improvement of visual quality
  - patterns for adaptive detail adaptation of geometry or textures

- DFG: 1 doctoral researcher, 1 student assistant

³http://univis.uni-erlangen.de → Research projects → RAMP
Run-Time Support System for Invasive Computing

**Octo**

- borrowed from the designation of a creature that:
  i. is highly parallel in its actions and
  ii. excellently can adapt oneself to its environment
- the kraken (species *Octopoda*)
  - can operate in parallel by virtue of its eight tentacle
  - is able to do customisation through camouflage and deimatic displays and
  - comes with a highly developed nervous system
    - in order to attune to dynamic ambient conditions and effects

**POS**

- abbrv. for *parallel operating system*
  - an operating system that not only supports parallel processes
  - but that also functions *inherently parallel* thereby

DFG: 2.5 doctoral researchers, 1 research/3 student assistants

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4 http://univis.uni-erlangen.de → Research projects → iRTSS
Power-Aware Critical Sections

- scalable synchronisation on the basis of **agile critical sections infrastructure**
- load-dependent and self-organised change of protection against race conditions
- **linguistic support**
- preparation, characterisation, and capturing of declared critical sections
- automated extraction of critical sections
  - notation language for critical sections
  - program analysis and LLVM integration/adaptation
- **power-aware system programming**
  - mutual exclusion, guarded sections, transactions
  - dynamic dispatch of synchronisation protocols or critical sections, resp.
- **tamper-proof power-consumption measuring**
  - instruction survey and statistics based on real and virtual machines
  - energy-consumption prediction or estimation, resp.

**DFG:** 2 doctoral researchers, 2 student assistants

[^5]: [http://univis.uni-erlangen.de → Research projects → PAX](http://univis.uni-erlangen.de → Research projects → PAX)
## Multi/Many-Core Processor Pool

<table>
<thead>
<tr>
<th>faui4*</th>
<th>clock</th>
<th>cores per domain</th>
<th>domain</th>
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<td>logical</td>
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</tbody>
</table>

Budgeted acquisition: further $n$-core systems, transactional memory

- **OctoPOS** $n \geq 64$, in 2015
- **PAX** $n \geq 16$, in 2016, plus several multi-core micro-controllers