Concurrent Systems

Nebenläufige Systeme

XIII. Pickings

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Outline

Recapitulation
Concurrent Systems

Perspectives
Parallel Systems
Computing Equipment
Further Education
Latency Awareness in Operating Systems

- **latency prevention**
  - lock- and wait-free synchronisation
  - integrated generator-based approach
- **latency avoidance**
  - interference protection
  - race-conflict containment
- **latency hiding**
  - operating-system server cores
  - asynchronous remote system operation
- experiments with different operating-system architectures
  - process-/event-based and hardware-centric operating-system kernels
  - LAKE, Sloth
- DFG: 2 doctoral researchers, 2 student assistants

Coherency Kernel

- **event-based minimal kernel**
  - cache-aware main-memory footprint
  - hyper-threading of latent actions
- featherweight agreement protocols
  - overall kernel-level synchronisation
  - families of consistency kernels
- **problem-oriented consistency**
  - sequential, entry, release consistency
  - functional hierarchy of consistency domains
  - memory domains for NUMA architectures
- implementation as to different processor architectures
  - partial or total, resp. {in,}coherent shared memory
- DFG: 2 doctoral researchers (1 FAU, 1 BTU)
Run-Time Support System for Invasive Computing

Octo

- borrowed from the designation of a creature that:
  1. is highly parallel in its actions and
  2. excellently can adapt oneself to its environment

- the kraken (species Octopoda)
  1. can operate in parallel by virtue of its eight tentacle
  2. is able to do customisation through camouflage and deimatic displays and
  3. comes with a highly developed nervous system
    - in order to attune to dynamic ambient conditions and effects

POSS

- abbrv. for parallel operating system
  - an operating system that not only supports parallel processes
  - but that also functions inherently parallel thereby

- DFG: 2.5 doctoral researchers, 1 research/3 student assistants

Power-Aware Critical Sections

- scalable synchronisation on the basis of agile critical sections
  - infrastructure
    - load-dependent and self-organised change of protection against race conditions
  - linguistic support
    - preparation, characterisation, and capturing of declared critical sections
  - automated extraction of critical sections
    - notation language for critical sections
    - program analysis and LLVM integration/adaptation
  - power-aware system programming
    - mutual exclusion, guarded sections, transactions
    - dynamic dispatch of synchronisation protocols or critical sections, resp.
    - tamper-proof power-consumption measuring
      - instruction survey and statistics based on real and virtual machines
      - energy-consumption prediction or estimation, resp.

- DFG: 2 doctoral researchers, 2 student assistants

Latency- and Resilience-Aware Networking

- real-time capable network communication
  - transport channel for cyber-physical systems
  - predictable transmission latency
  - in a certain extent guaranteed quality criteria

- deterministic run-time support
  - Auffassung von der kausalen [Vor]bestimmtheit allen Geschehens bzw. Handelns (Duden)

  - latency-aware communication endpoints, optimised protocol stack
    - in time (phase 1) and energy (phase 2) respect

- DFG: doctoral researchers, 2 student assistants (1 FAU, 1 Uni SB)

Multi/Many-Core Processor Pool

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