Concurrent Systems

Nebenläufige Systeme

XIV. Pickings

Wolfgang Schröder-Preikschat

February 11, 2021
Agenda

Recapitulation
  Concurrent Systems

Perspectives
  Parallel Systems
  Computing Equipment
  Further Education
Recapitulation

Concurrent Systems

Perspectives

Parallel Systems
Computing Equipment
Further Education
# Content of Teaching and Cross-References

<table>
<thead>
<tr>
<th>BS</th>
<th>HBS</th>
<th>ParAlg</th>
<th>PFP</th>
<th>TRASYS</th>
</tr>
</thead>
<tbody>
<tr>
<td>concurrency</td>
<td>simultaneous (concurrent/interacting) processes</td>
<td>critical sections</td>
<td>elementary operations</td>
<td></td>
</tr>
<tr>
<td>lock</td>
<td>semaphore</td>
<td>monitor</td>
<td>deadly embrace</td>
<td>non-blocking synchronisation</td>
</tr>
</tbody>
</table>

© wosch, CS (WS 2020/21, LEC 14) Recapitulation – Concurrent Systems
Outline

Recapitulation
Concurrent Systems

Perspectives
Parallel Systems
Computing Equipment
Further Education
Main Research at the Chair

- **composability** and **configurability**
  - application-oriented (varying, type-safe) system software

- **specialisation**
  - dedicated operating systems: integrated, adaptive, parallel

- **reliability**
  - gentle fault and intrusion tolerance

- **thriftiness**
  - resource-aware operation of computing systems

- **timeliness**
  - migration paths between time- and event-triggered real-time systems

- **concurrency**
  - coordination of cooperation and competition between processes

"concurrent systems" is more or less **cross-cutting** thereto...
Latency Awareness in Operating Systems

- **latency prevention**
  - lock- and wait-free synchronisation
  - integrated generator-based approach

- **latency avoidance**
  - interference protection
  - race-conflict containment

- **latency hiding**
  - operating-system server cores
  - asynchronous remote system operation
  - experiments with different operating-system architectures
    - process-/event-based and hardware-centric operating-system kernels
    - LAKE, Sloth

- DFG: 2 doctoral researchers, 2 student assistants

---

1. http://univis.uni-erlangen.de → Research projects → LAOS
Coherency Kernel

- **event-based minimal kernel**
  - cache-aware main-memory footprint
  - hyper-threading of latent actions

- **featherweight agreement protocols**
  - overall kernel-level synchronisation
  - families of consistency kernels

- **problem-oriented consistency**
  - sequential, entry, release consistency
  - functional hierarchy of consistency domains
  - memory domains for NUMA architectures

- implementation as to different **processor architectures**
  - partial or total, resp. \{in,\}coherent shared memory

- DFG: 2 doctoral researchers (1 FAU, 1 BTU)

\[2\text{http://univis.uni-erlangen.de → Research projects → COKE}\]
Power-Aware Critical Sections

- scalable synchronisation on the basis of agile critical sections infrastructure
  - load-dependent and self-organised change of protection against race conditions

- linguistic support
  - preparation, characterisation, and capturing of declared critical sections

- automated extraction of critical sections
  - notation language for critical sections
  - program analysis and LLVM integration/adaptation

- power-aware system programming
  - mutual exclusion, guarded sections, transactions
  - dynamic dispatch of synchronisation protocols or critical sections, resp.

- tamper-proof power-consumption measuring
  - instruction survey and statistics based on real and virtual machines
  - energy-consumption prediction or estimation, resp.

- DFG: 2 doctoral researchers, 2 student assistants

³http://univis.uni-erlangen.de → Research projects → PAX
Latency- and Resilience-Aware Networking

- **real-time capable network communication**
  - transport channel for cyber-physical systems
  - predictable transmission latency
  - in a certain extent guaranteed quality criteria

- **deterministic run-time support**
  
  Auffassung von der kausalen [Vor]bestimmtheit allen Geschehens bzw. Handelns (Duden)

- latency-aware communication endpoints, optimised protocol stack
- specialised resource management, predictable run-time behaviour
  - in time (phase 1) and energy (phase 2) respect

- DFG: doctoral researchers, 2 student assistants (1 FAU, 1 Uni SB)

---

[^4]: [http://univis.uni-erlangen.de → Research projects → LARN](http://univis.uni-erlangen.de → Research projects → LARN)
Run-Time Support System for Invasive Computing

Octo

borrowed from the designation of a creature that:

i. is highly parallel in its actions and
ii. excellently can adapt oneself to its environment

the kraken (species Octopoda)

- can operate in parallel by virtue of its eight tentacle
- is able to do customisation through camouflage and deimatic displays and
- comes with a highly developed nervous system
  - in order to attune to dynamic ambient conditions and effects

POS

abbrv. for parallel operating system

- an operating system that not only supports parallel processes
- but that also functions inherently parallel thereby

DFG: 2.5 doctoral researchers, 1 research/3 student assistants

\[\text{http://univis.uni-erlangen.de} \rightarrow \text{Research projects} \rightarrow \text{iRTSS}\]
## Multi/Many-Core Processor Pool

<table>
<thead>
<tr>
<th>faui4*</th>
<th>clock</th>
<th>cores per domain</th>
<th>domain</th>
<th>#</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>physical</td>
<td>logical</td>
<td>NUMA</td>
</tr>
<tr>
<td>*8e</td>
<td>2.9 GHz</td>
<td>8</td>
<td>16</td>
<td>2</td>
</tr>
<tr>
<td>*8f</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>*9big01</td>
<td>2.5 GHz</td>
<td>6</td>
<td>6</td>
<td>8</td>
</tr>
<tr>
<td>*9big02</td>
<td>2.2 GHz</td>
<td>10</td>
<td>20</td>
<td>4</td>
</tr>
<tr>
<td>*9big03</td>
<td>2.1 GHz</td>
<td>12</td>
<td>24</td>
<td>4</td>
</tr>
<tr>
<td>*9big04</td>
<td>2 GHz$^6$</td>
<td>64</td>
<td>128</td>
<td>2</td>
</tr>
<tr>
<td>*9big05</td>
<td>2.5 GHz</td>
<td>16</td>
<td>128</td>
<td>2</td>
</tr>
<tr>
<td>*9phi01</td>
<td>1.2 GHz</td>
<td>6</td>
<td>12</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>1.1 GHz</td>
<td>57</td>
<td>228</td>
<td>2</td>
</tr>
<tr>
<td>*scc</td>
<td>1.5 GHz</td>
<td>4</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>800 MHz</td>
<td>2</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>fastbox</td>
<td>3.5 GHz</td>
<td>4</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>InvasIC</td>
<td>50 MHz</td>
<td>5</td>
<td>5</td>
<td>16</td>
</tr>
</tbody>
</table>

$^6$ mit *boost* 3.35 GHz

© wosch
CS (WS 2020/21, LEC 14) Perspectives – Computing Equipment 12
Bachelor, Master, or Doctoral Thesis